

Methodology to standardize the development of FPGA-based intelligent DAQ and processing systems on heterogeneous platforms using OpenCL

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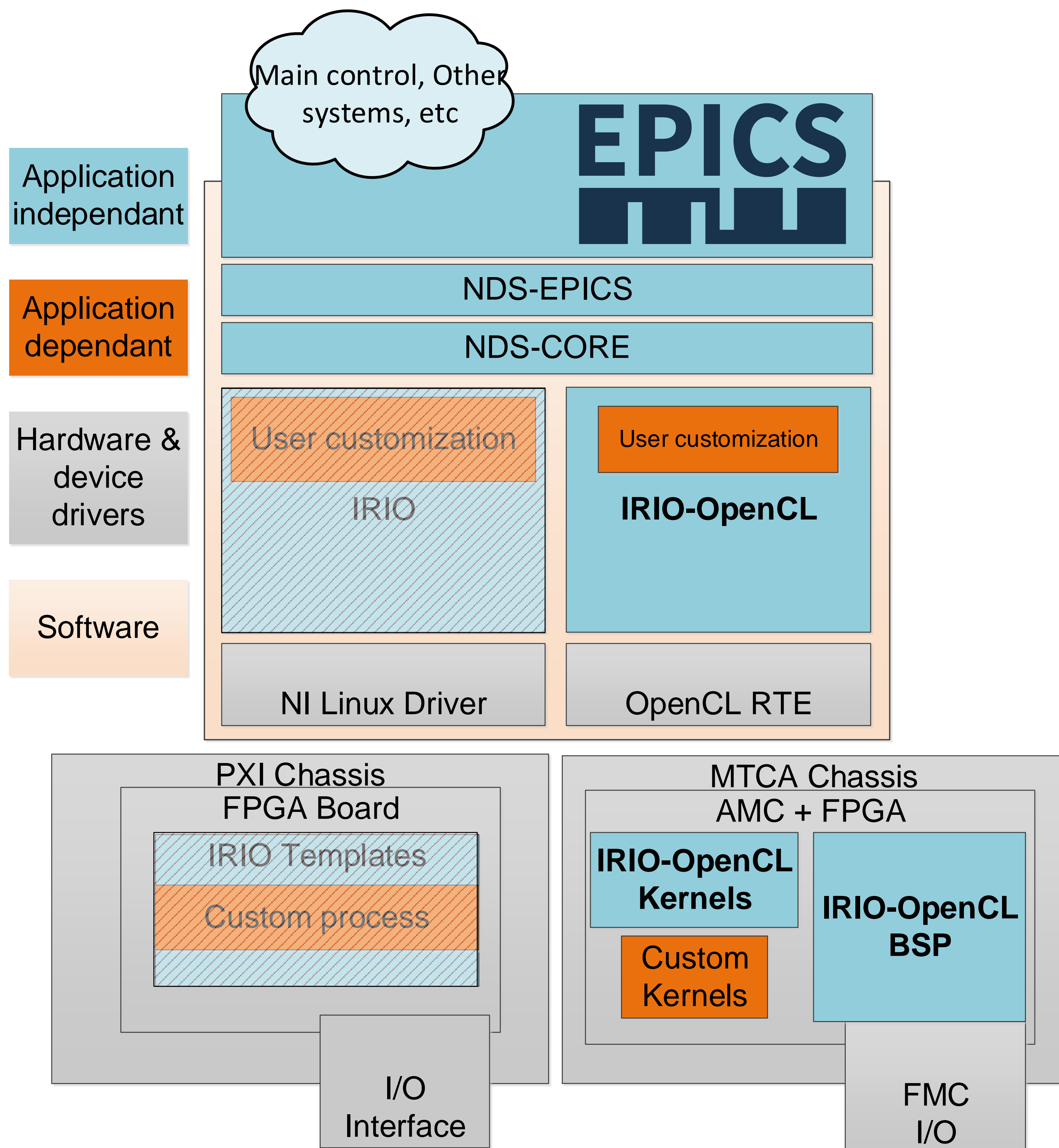
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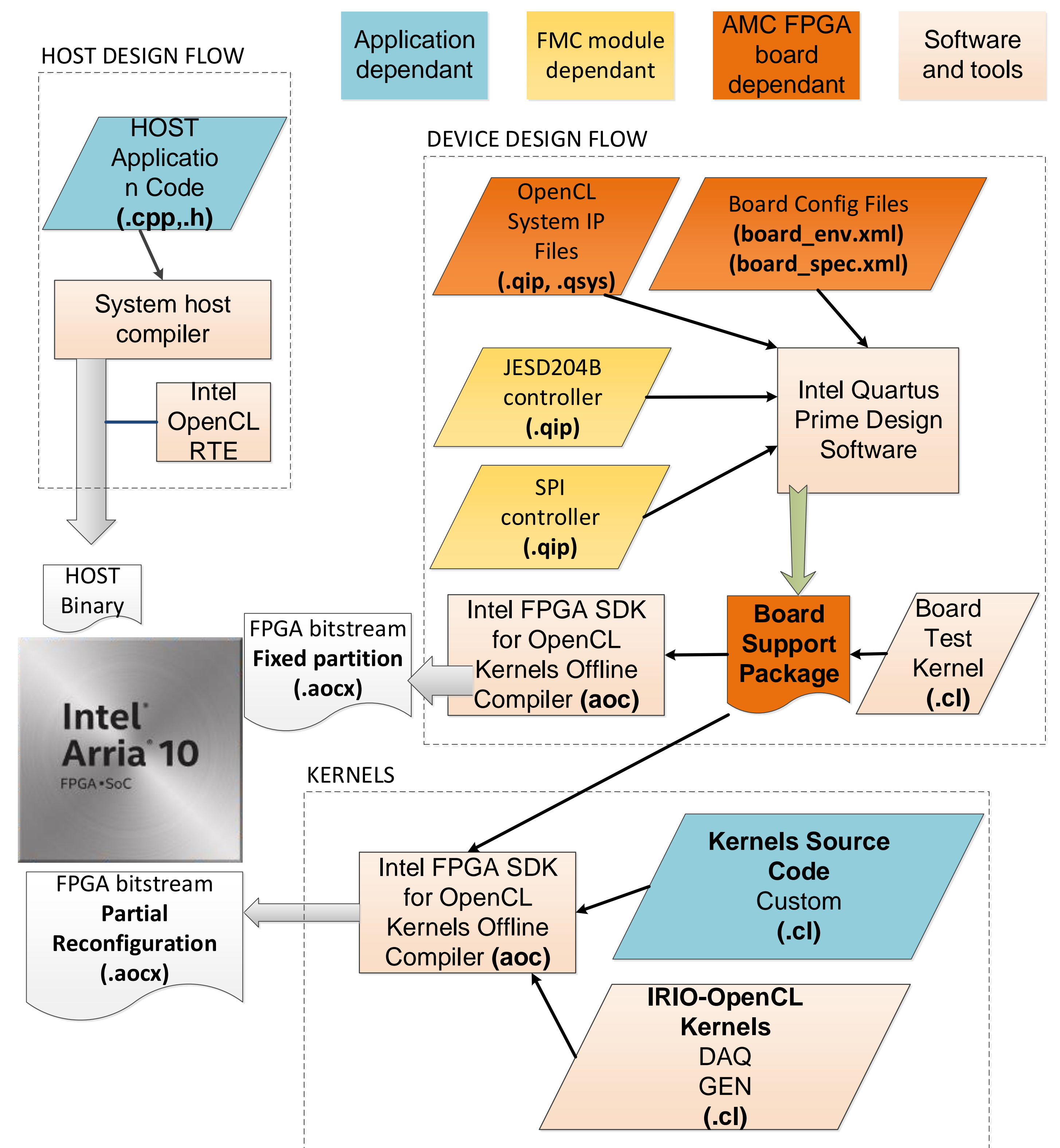
BACKGROUND

- Design cycles for FPGA based applications are still complex and costly.
- IRIO was developed for the PXI platform, mainly FlexRIO and cRIO.
- Standardization adds value to high-level languages, reducing the development times, by reusing existing code.
- OpenCL opens to new manufacturers and heterogeneous devices.

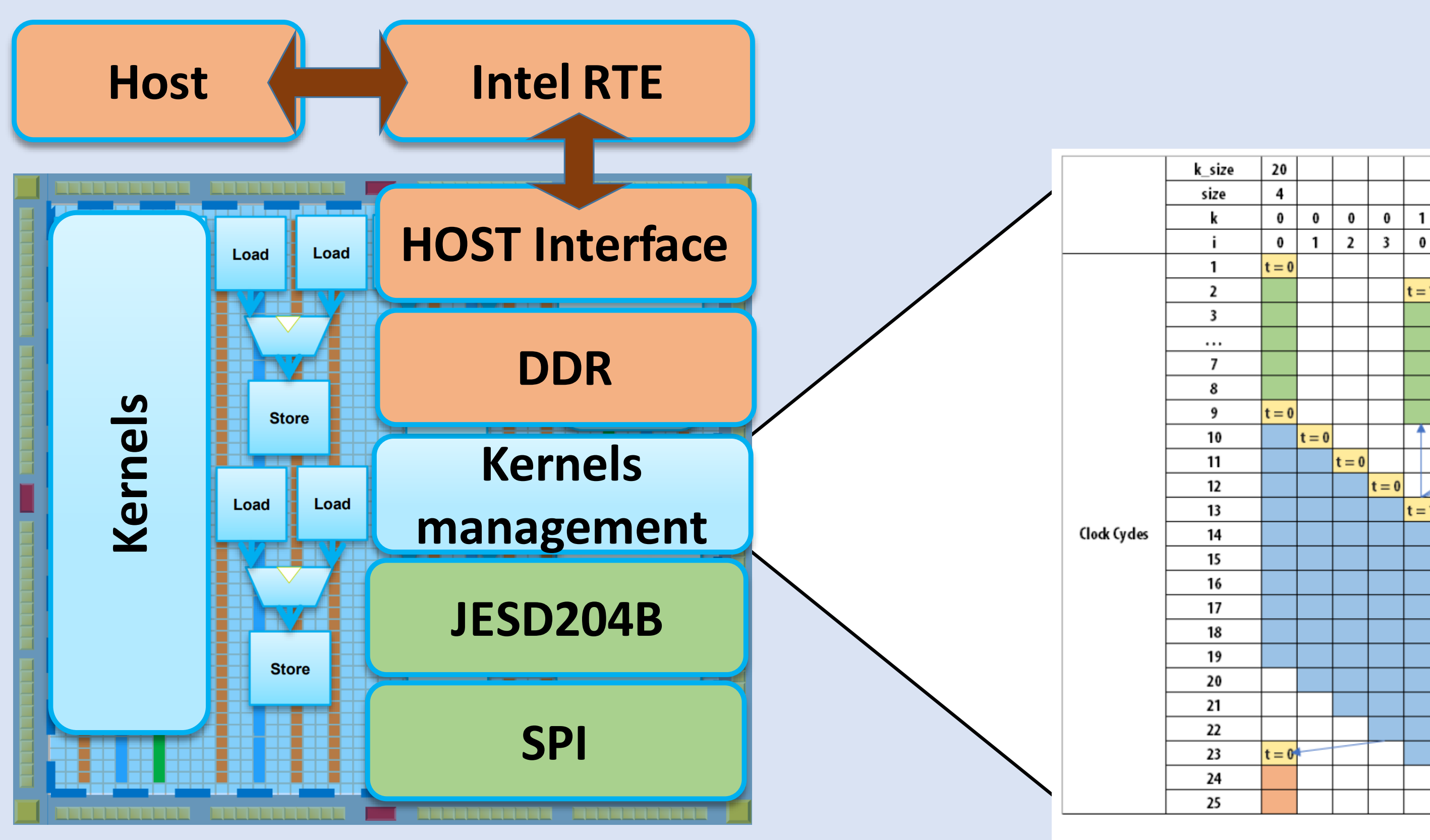


METHODS

- NDSV3 supports hardware functionality on a tree like structure of nodes. By creating IRIO-OpenCL kernels and host code we can recreate this functionality on the FPGA.
1. Changing processing algorithms is easy. (Blue)
 2. Changes to I/O hardware requires minor changes. (Yellow)
 3. AMC FPGA Board changes require BSP porting. (Orange)



IMPLEMENTATION



- OpenCL is built as a parallel computing language.
- It uses C/C++ code and a robust memory model.
- **Parallelism** on the FPGA is costly on area, it is rather achieved by pipelining the **Kernels** to generate a very fast stream of data.
- The board support package (**BSP**) contains all the necessary hardware to manage **DDR, JESD204B, Host PCIe and memory interface, ...** and kernels execution.

CONCLUSION

- With IRIO-OpenCL kernels, DAQ functionality is resolved so that the scientists can focus only on the processing algorithms.
- FPGA development can be reduced by using OpenCL which works well with standardization software like NDSv3.
- By combining these techniques, very demanding algorithms can be deployed to specialized hardware with the minimum effort.

ACKNOWLEDGEMENTS

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