Design and Development of a Cost Optimized Timing System for Steady State Superconducting Tokamak (SST-1)

J. DHONGDE, A. Kumar, D. Raju & SST-1 Operations Division
Institute for Plasma Research
jasraj@ipr.res.in

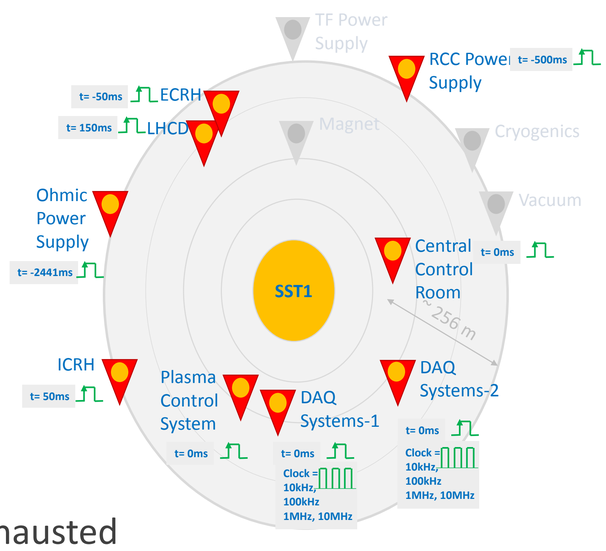
ID: 443

ABSTRACT

- SST-1 timing system is a **real time event based trigger generation and distribution system** used for the synchronized operation of its various heterogeneous and distributed sub-systems during the plasma discharges.
- A **platform independent, stand alone, 1U rack mountable timing system** is designed, developed and tested based on Xilinx's Artix-7 FPGAs for real time event (trigger) distribution amongst different subsystems of SST-1.
- Timing system modules are designed using **Xilinx's Artix-7 FPGA** for the programmable resources like RAM, DPRAM using IP cores, implementation of glue-logic timing as well as implementation of serialization-deserialization logic based on asynchronous serial communication protocol for event (trigger) information distribution over fiber optic network.
- In this new system, **single central timing system** module can support an interface of maximum of **eight (8) subsystem modules in star configuration over optical fiber network**.
- The central timing system module can generate pre-defined **experiment event (trigger) sequence in real time with a resolution of 10µs** and facilitates **event logging at a resolution of 1µs**.Each sub-system module can support **eight (8) TTL inputs for asynchronous event generation and eight (8) TTL outputs** for trigger pulse generation with a resolution of 1µs.
- **Event latency is observed to be in the range of ~ 4µs** over 3m length of optical fiber cable

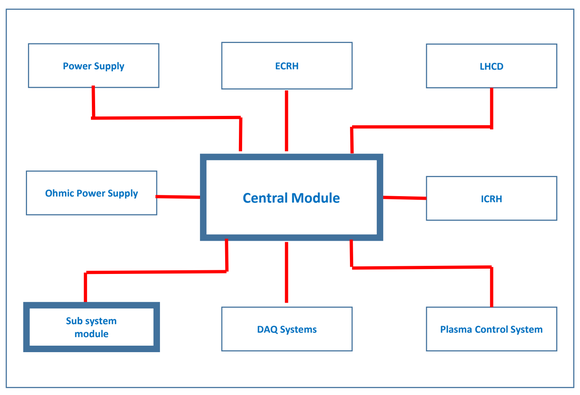
OLD TIMING SYSTEM

- Based on **VME Platform** (~ 15Years). Custom VME Timing System cards were in house designed and developed.
- **Master – Slave configuration** connected in star configuration. Optical Network – **Multimode, 62.5/125 µm**.
- Provide fast timing signals **(clock & triggers)** to various sub systems during plasma discharges

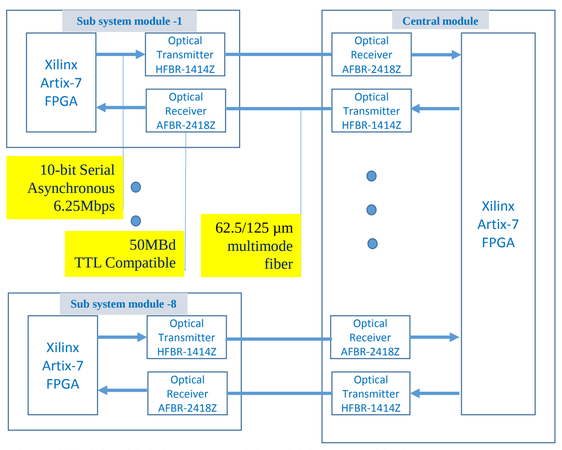


- Timing System card inventory got exhausted
- Sub system hardware advancement also started (Systems migrated from VME to PXI, PXIe etc.)

NEW TIMING SYSTEM

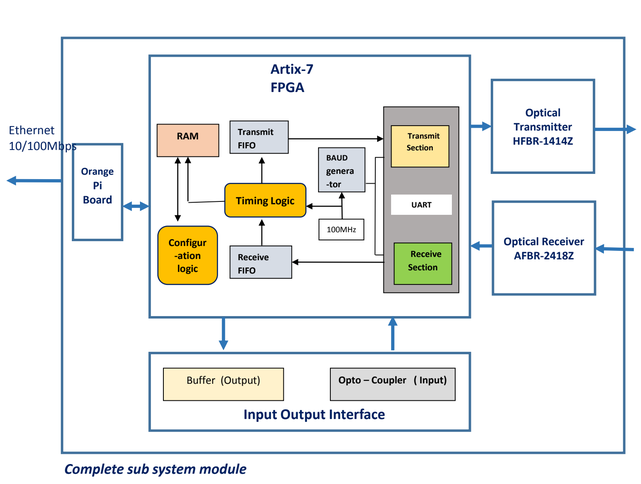


Simple block diagram – Central Module with Sub system modules in star topology



Central Module with Sub system modules with important blocks

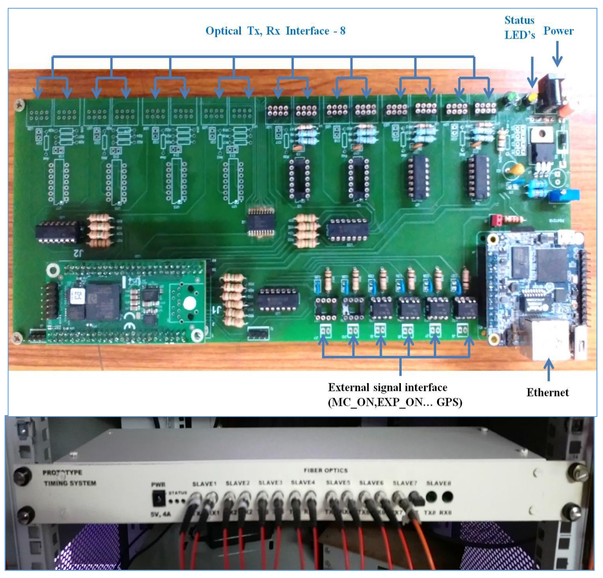
- A platform independent
- Standalone,
- 1U Rack mountable modules
  - Central module
  - Sub system module
- Connected in star configuration. Optical Network – Multimode, 62.5/125 µm
- Provide real time event (trigger) distribution to various sub systems during plasma discharges (version1)
- Modules designed using Xilinx's Artix-7 FPGA



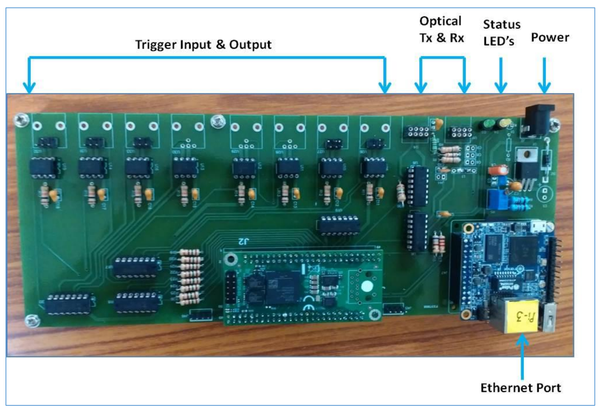
Complete sub system module

Note : Central module – additional Multiple Transmitter and receiver sections are present.

NEW TIMING SYSTEM BOARDS (Version1)



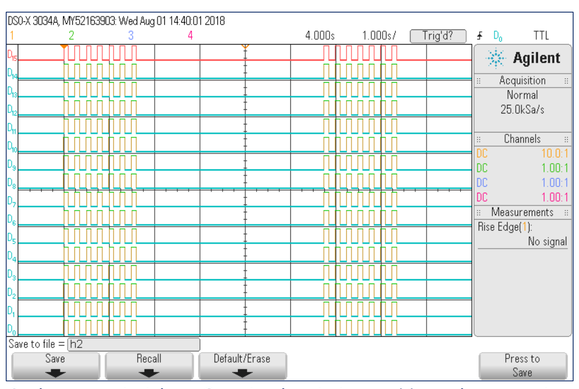
- Maximum Slave modules that can be connected = 8
- Synchronous & Shut down sequence event time resolution = 10 µS
- Event time stamp resolution = 1µs
- Maximum number of synchronous & shut down sequence events = 255
- Maximum event time stamp duration = 4294.96s (~ 71.58 min)
- **Cost Estimated** = Rs. 41,698 /- approx. (600$)



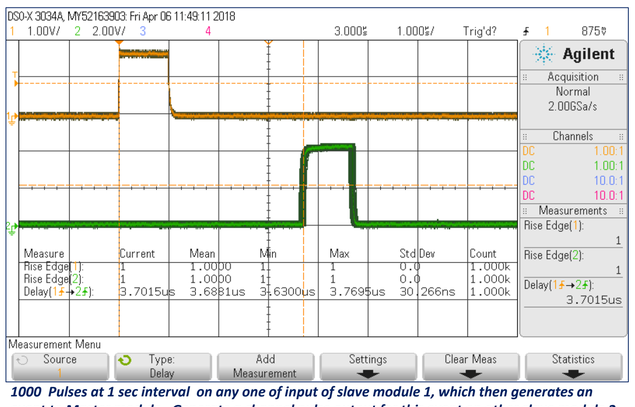
- TTL Channel Outputs = 8 (Low to High)
- TTL Channel Inputs = 8 (Rising edge i.e. low to high logic)
- Minimum pulse width for channel outputs = 1µS
- Maximum pulse width for channel output = 429.49 sec
- Minimum pulse width at channel input = 500ns (as event)

Cost Estimated = Rs. 25,168 /- approx. (360$)

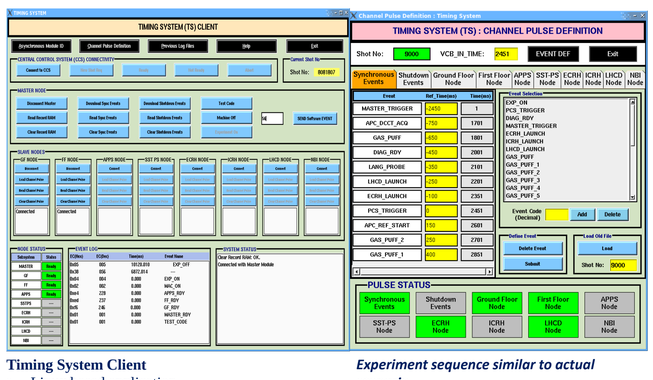
PERFORMANCE,RESULTS & VALIDATION



Synchronous events at slaves- Generate pulse outputs on receiving synchronous events (7x8) and shutdown events (7x8) on all eight outputs of two different slave modules
D0-D7 : Sub system1 outputs
D8-D15 : Sub system 2 outputs

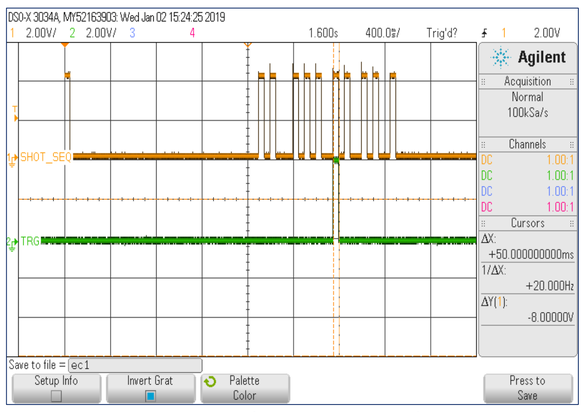


1000 Pulses at 1 sec interval on any one of input of slave module 1, which then generates an event to Master module. Generate a channel pulse output for this event on other slave module 2.
Ch1: Pulse input also observed on oscilloscope (as an input to sub system module 1)
Ch2: Output generated on sub system module 2 by the corresponding event generated due to above pulse input



Timing System Client
- Linux based application
- Client-Server architecture
- Connects & Configures all Timing System modules
- Issues commands to generate experiment sequences
- Online event information to operator

Experiment sequence similar to actual scenario



Real time event sequence generation (ECRH Launch trigger in reference to actual plasma shot scenario)

SUMMARY

- A Platform independent, stand alone, 1U rack mountable timing system is designed, developed and tested.
- The performance test results are comparable and acceptable.
- The development cost is observed to be optimized considering the simple design adopted.
- Design can be implemented with other FPGAs (different make)
- New in-house design will be advantageous and it can be easily adapted for time synchronization applications in small, medium size tokamaks or experimental devices irrespective of hardware/ software platforms.

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