The Implementation and operation of the 4th version of the KSTAR Fast Interlock System

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ABSTRACT

- 4th version of KSTAR Fast Interlock System (FIS) using NI c-RIO technology built and operated in 2018.
- The EPICS irio driver enables complete control and monitoring of the FPGA, and the distributed interlock information can be integrated in the FIS IOC via EPICS.
- The FPGA, which is responsible for signal processing at high speed, implements the event counter logic to record the event occurrence time.
- The event generated in the FPGA is displayed in 10 microseconds resolution by the 100 kHz operation period.

INTRODUCTION

History of KSTAR FIS [1], [2]

- 1st Version, 2009 : Central Control System + Plasma Control System using RFM within 200ms
- 2nd Version, 2012 : Fast interlock interface + TSS
- 3rd Version, 2014 : 2nd Version + PFC, NB armor temp. faults
- 4th Version, 2018 : c-RIO+EPICS IOC

FIS protection logics [3]

- Ip protection logic : FPGA processing
- PCS, SIS interface logic : information transfer using hardware
- EPICS PV interface logic : information transfer using EPICS PV

IMPLEMENTATION

FPGA Implementation

- Labview FPGA module, EPICS irio driver [4]
- 4 execution loops (Ip logic, Event count, heating stop, heart-beat check)
- Timing sync. With KSTAR TSS

OPI

- Using EPICS Control System Studio(CSS)
- Linked with KSTAR shot based operation

OPERATION and RESULTS

Reset and Clear faults

- Pulse Automation and Shot Scheduling(PASS), PCS, Timing interfaced FPGA logic.
- Least operator’s intervention.

Performance Evaluation

- Focus on start-up phase (<250ms)
- Analysis on Ip profile and Heating Stop(HS) time
- Event counter value converted to Blip based discharge time.
- 100kHz Ip protection logic perfectly working and generated HS signal.
- Case1, case2 shows perfect working.

CONCLUSION

- 4th version of KSTAR FIS worked without any problem during 2018 operation.
- Using FPGA event counter logic, FIS performance evaluation was done.
- Event counter was very useful to specify the error/fault source.
- The level of Ip threshold should be reviewed and another protection logics can be added for the FIS upgrade.

REFERENCES

4. “IRIO EPICS device support-V1.2.0 user’s manual”, UPM, Spain