Progress in High Power Test of R&D Source for ITER ICRF system

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Outline

ITER ICRF System

- Functional Requirements & Layout

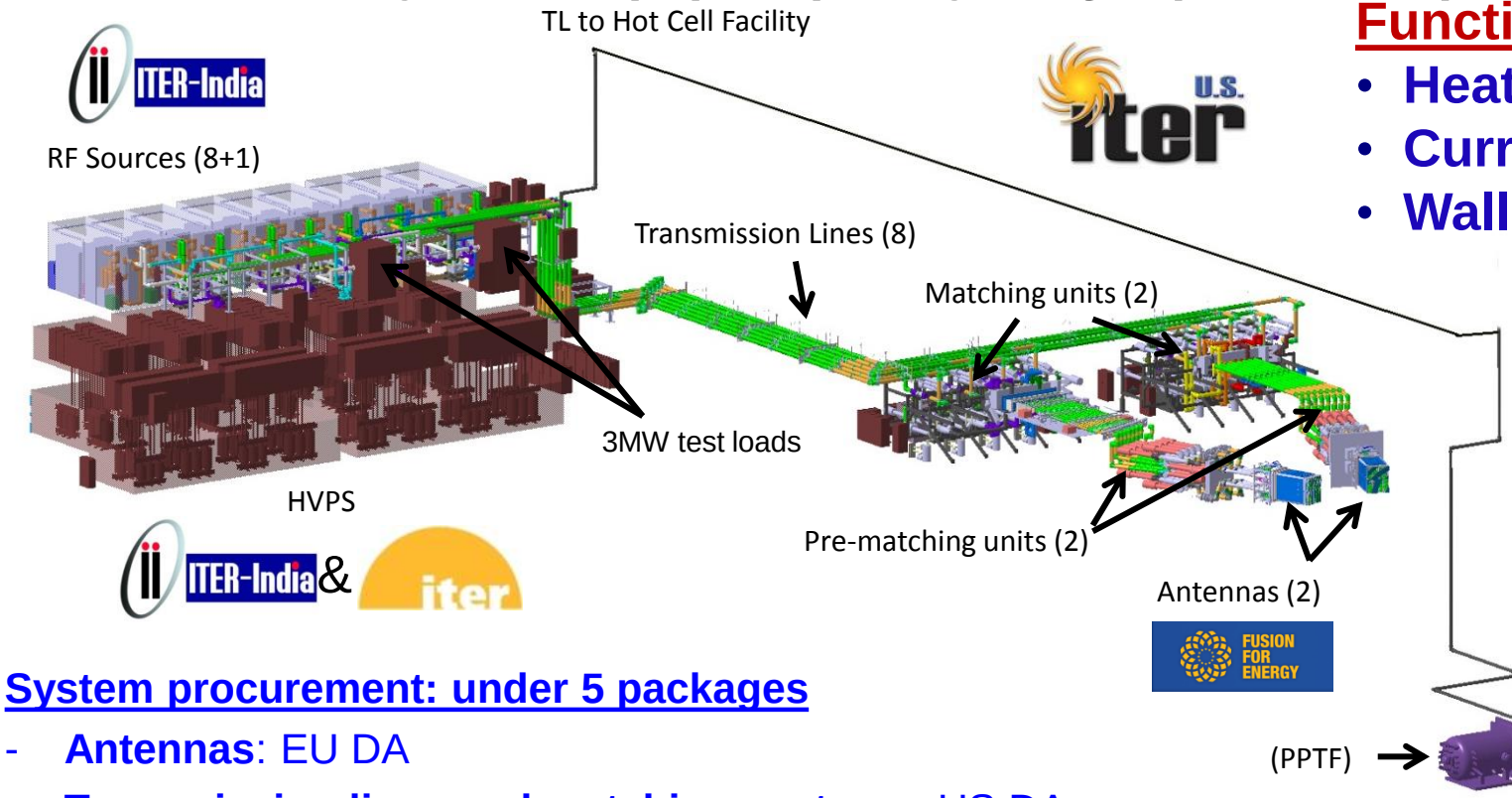
ICRF Source System

- Major Specifications & Technical Challenges Involved
- R&D activity: Development of Diacrode Based System
  - RF Amplifiers, Controls, High Power Test Rig
  - Commissioning results
    - ❑ Matched Load Condition
    - ❑ Mismatched Load Condition

Summary

ITER ICRF System

ITER requires 20MW of RF power to a variety of plasmas in Ion Cyclotron (IC) frequency range (40-55 MHz)



Functionality:

- **Heating**
- **Current drive**
- **Wall conditioning**

System procurement: under 5 packages

- **Antennas**: EU DA
- **Transmission lines and matching systems**: US DA
- **RF sources:** IN DA
- **HV Power Supplies**: IN DA + IO (part of HVPS)
- **Plant Control System:** IO

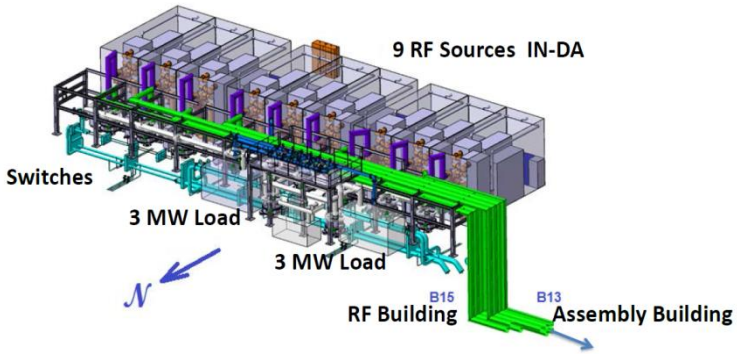
Each antenna will be fed by 4 number of RF sources connected with 8 transmission lines & associated matching units

ICRF Source System

IN Commitment : 9 nos. of RF sources (8 for plasma operation + 1 spare)

Major Specifications

- **Each source will have**
  - **Power handling capability:**
    - **2.5 MW at VSWR 2.0 / 35-65 MHz/CW**
    - **3.0 MW at VSWR 1.5 / 40-55 MHz/CW**
  - **Power modulation range: 2 kW – 2.5 MW**
  - **Freq. deviation over any central freq.: ± 1 MHz (1 dB)**
  - **Transient VSWR (for 1 s): 2.5**
  - **η : 45% (mismatched load condition) – 65%(matched load condition)**
  - **Harmonic level: <-20 dBc & Emergency shutdown: <10 μ sec**



As there is no unique amplifier chain able to meet the output power specifications as per ITER need, ITER-India proposed a layout consists of two parallel three-stage amplifier chains + a combiner circuit on the output side

This kind of RF source is unique in terms of its stringent specifications

Technical Challenges Involved

- Combined high power & high VSWR are challenging, even for single chain of amplifiers
- CW aspect of the operation (efficient thermal management)
- Broad frequency range associated with BW (± 1 MHz at 1 dB point)
- Operational problems like, settling time of anode voltage, excess anode dissipation etc., during mismatch situation
- Unwanted oscillation & mode generation during operation

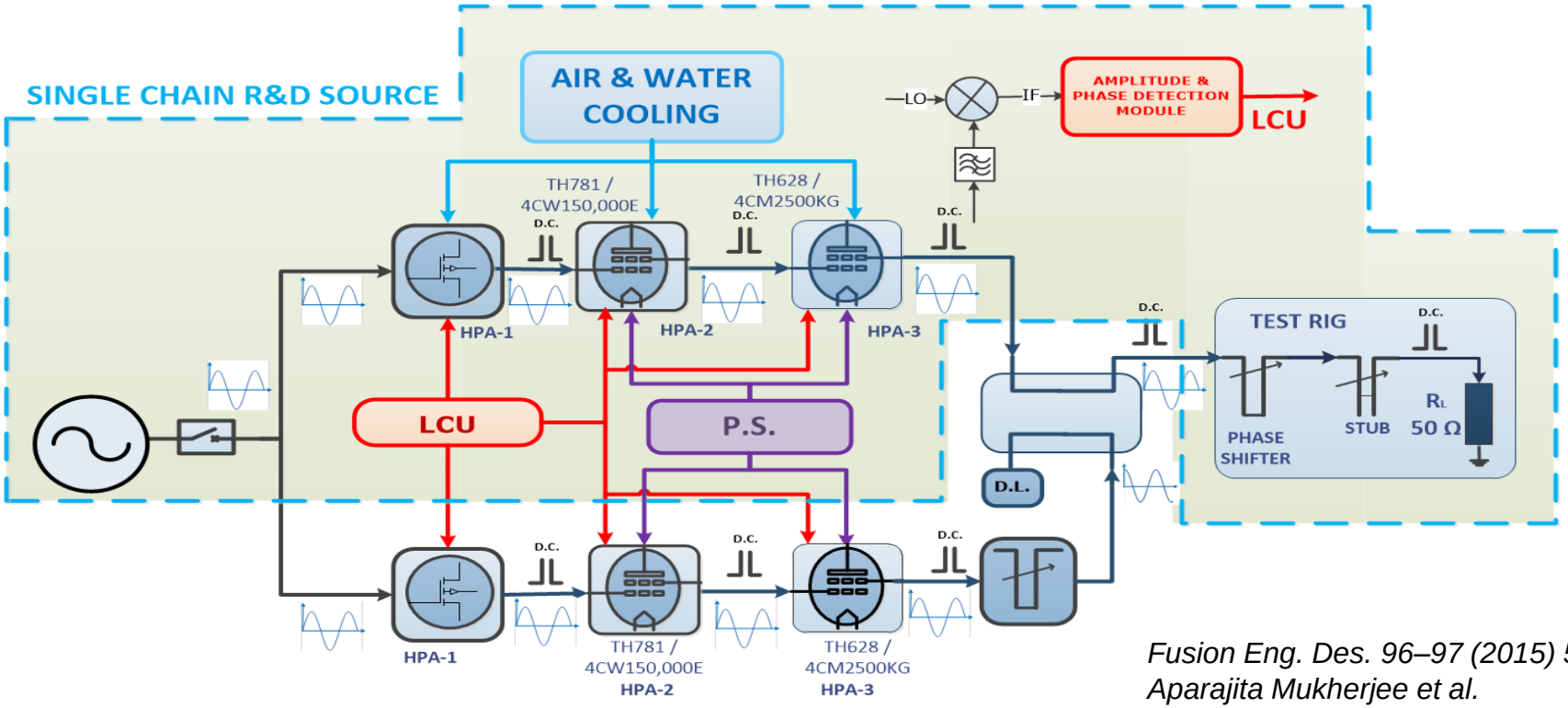
To address major issues: Tube qualification phase using single chain (R&D) experimentation 1.5 MW / 3600s / 35 - 65 MHz at VSWR 2.0 with any phase of reflection coefficient launched

State of the art at the start of R&D

ITER Specification	CPI, USA (Tetrode)	Thales, France (Diacrode)
2.5 MW/VSWR 2:1/ 2000s	~1.9 MW/VSWR 1:1/300s	1 MW/VSWR 1:1/1000 hrs.
η ~ 50% - 60%	> 60 %	> 60%
F = 35 – 65 MHz	30 – 60 MHz	200 MHz
BW:±1MHz at 1dB	High Q cavity	High Q cavity

R&D activity

- **Exploration of capabilities for Tetrode & Diacrode as final stage tube (collaborative contract launched with Thales, France & CEC, USA)**
- **Tubes and cavities are integrated in a full amplifier chain developed by ITER-India**
- **Tests under ITER specifications validates each design**



Fusion Eng. Des. 96–97 (2015) 542, Aparajita Mukherjee et al.

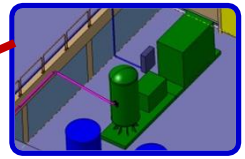
Test facility at ITER-India lab

Power supply	FPS	CGPS	SGPS
HPA2	0-10V DC/400A	0 to -500V DC/1.5A	0-2kV/2A
HPA3	0-20V DC/1200A	0 to -500V DC/6A	0-2kV/8A

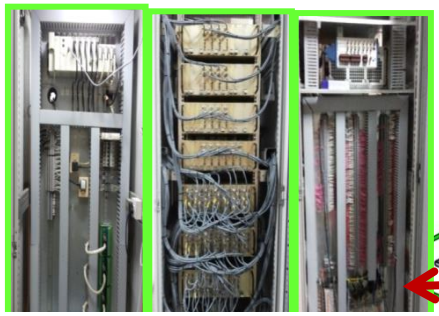
LP section

SSPA

Aux. PS



3MW Tx-line



PLC & PXI based Controls

Test Bed

Cooling dist. system

HVPS

3MW DL

MMTL

- Output V/I:14-18kV,10-15A (HPA2); 16-27kV,105-160A (HPA3)
- Accuracy, Resolution and Ripple: ± 1 %, 100 Volts, ± 1 %
- Energy Dumped: less than 10J, Rise time: 100 μs to 5ms

R&D activity using Diacrode technology

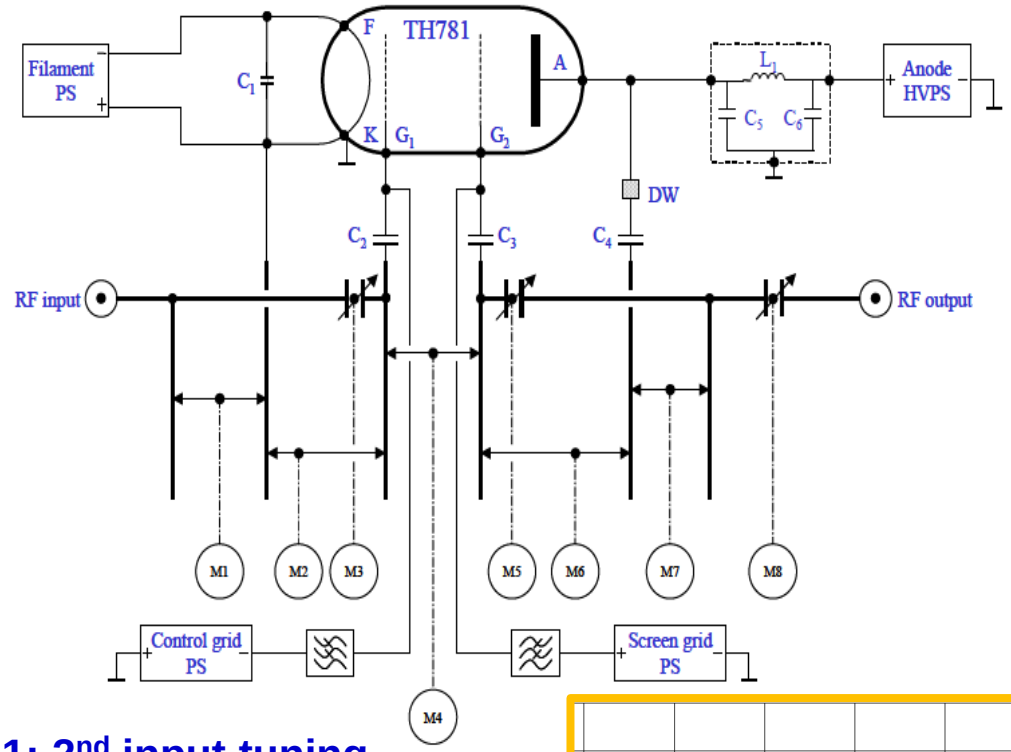
Chain of RF Amplifier

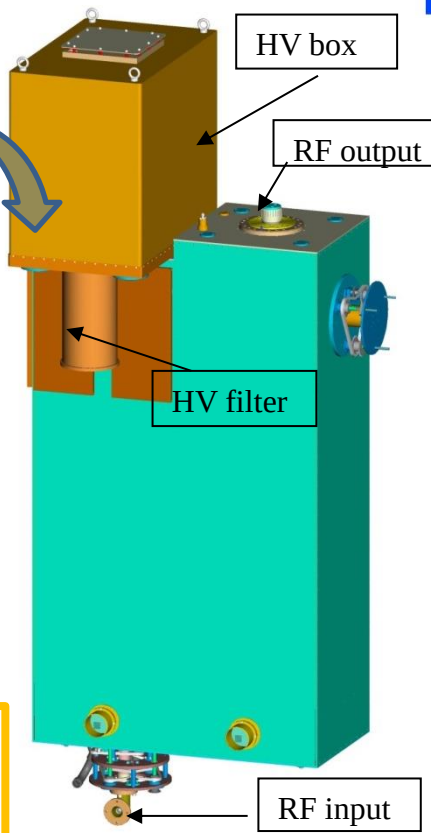
Amplification: mW to MW ⟹ ~ 90 dB gain

RF chain consists of:

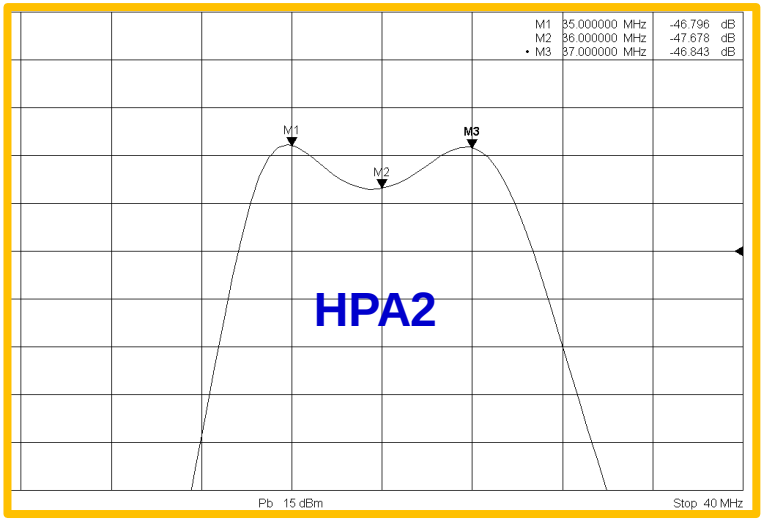
- Low power RF section **(mW)** + wide band pre-driver **(10kW SSPA)** + two tube based amplifiers: **130kW driver stage** (HPA2) & **1.5 MW final stage** (HPA3)
- Selected tubes:
  - **for HPA2: Tetrode TH781**
  - **for HPA3: Diacrode TH628L**
- Common grid configuration selected to provide stable operation
- Input & output cavities: tunable coaxial structures to provide impedance transformation for the required frequency range
- Coaxial structure provides
  - ✓ low spurious,
  - ✓ Low losses
  - ✓ natural EMI shielding
- Since tubes can oscillate at higher order modes, damping material is used to suppress them

RF Amplifier HPA2





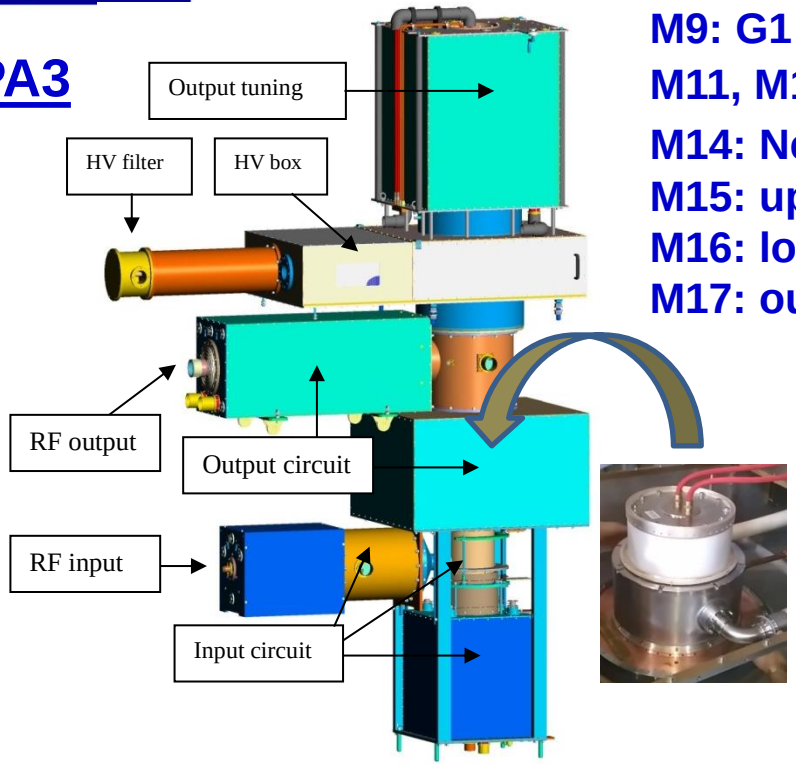
M1: 2nd input tuning
M2: 1st input tuning
M3: input coupling
M4: Neutralization
M5: primary to secondary output coupling
M6: primary output tuning
M7: secondary output tuning
M8: output coupling



Transmission characteristics at 36 MHz

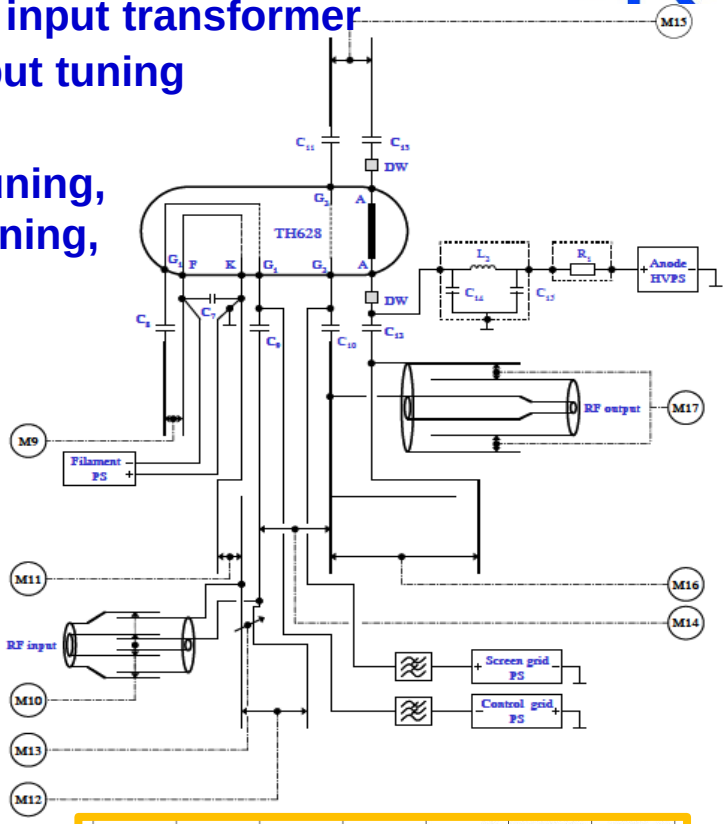
RF Amplifier HPA3

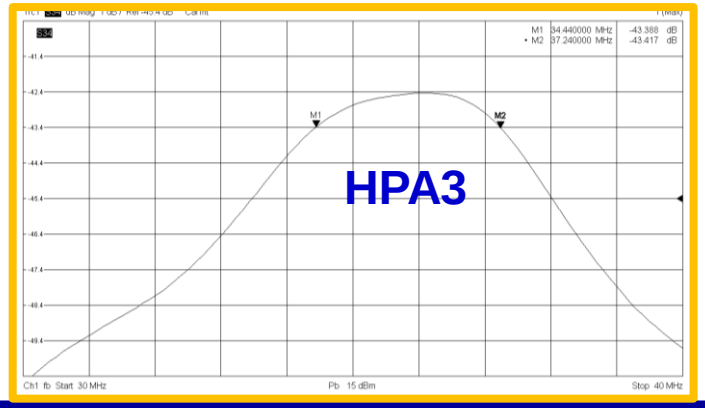
HPA3



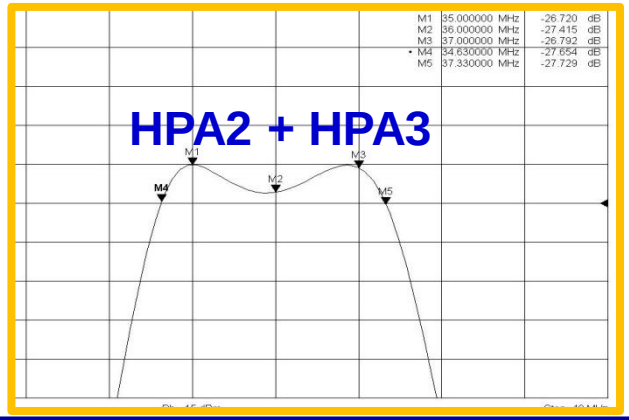
M9: G1 tuning, M10: input transformer
M11, M12 & M13: input tuning
M14: Neutralization,
M15: upper anode tuning,
M16: lower anode tuning,
M17: output tuning

Variable 6" Phase Shifter is placed in between HPA2 & HPA3 to get rid of any side effects





Transmission characteristics at 36 MHz



Controls

PLC based

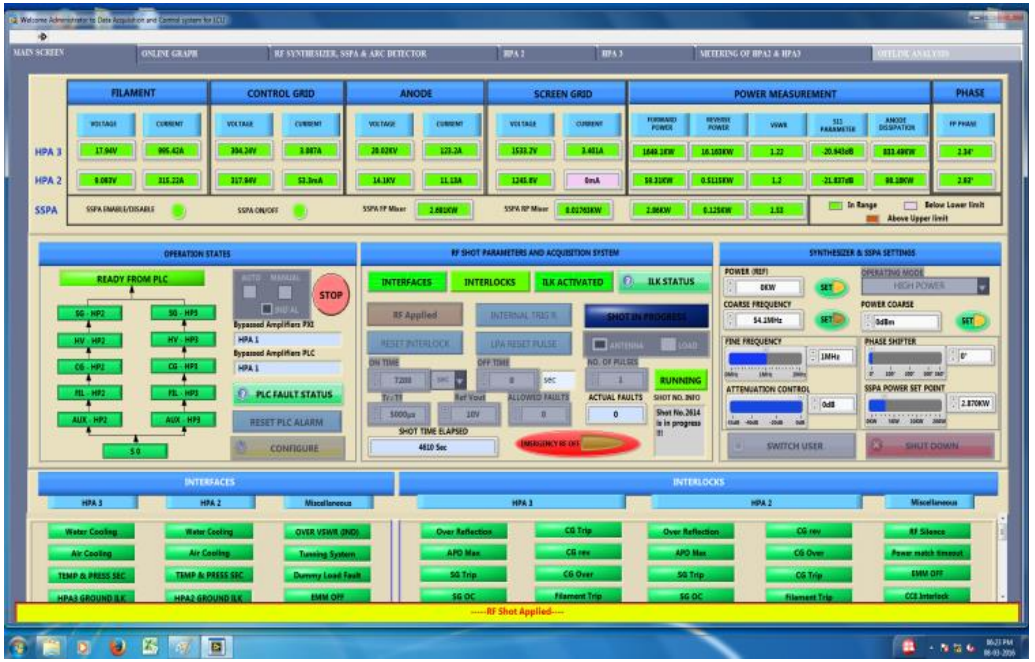
Sequence control system

PXI based

Real Time (RT) control, Interlocks, Acquisition & Display

Feedback control loops:

- Anode voltage loop to regulate Va for optimization of P_{dis} & SG_{dis}
- VSWR loop for making constant load power



To protect RF source against critical fault condition, local protection logic developed ensuring fast shut off (<10μs) of RF & power supplies

Data acquisition:

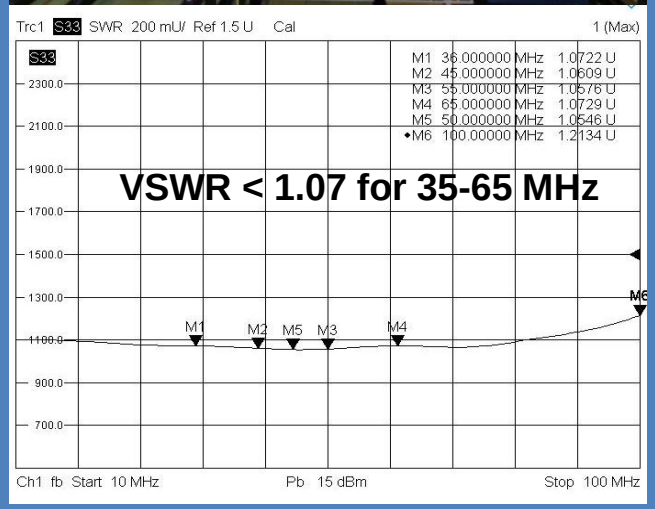
- 40 channel continuous at 1 kHz sampling frequency
- Event driven with 100 ms pre-post data at 1MHz sampling frequency

- Any selected 8 channel data of 100 sec duration at 1 kHz sampling frequency can be displayed on online graph.
- Loggings as well as display of user selectable channels for fault/offline analysis

High Power Test Rig

Capability: 3MW/3600s/35-65 MHz, up to VSWR 3:1 at all reflection angles

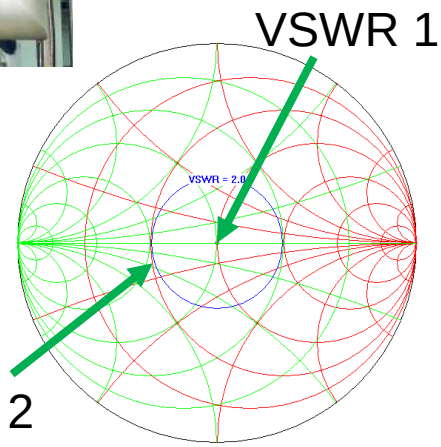
Test on Match load: RF power dumped on DL



Test on Mismatch load: RF power dumped on DL via MMTL system

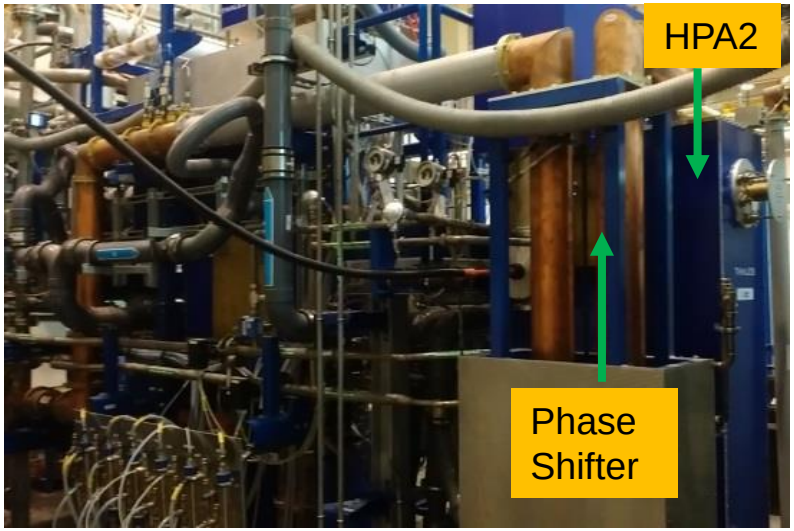
\+

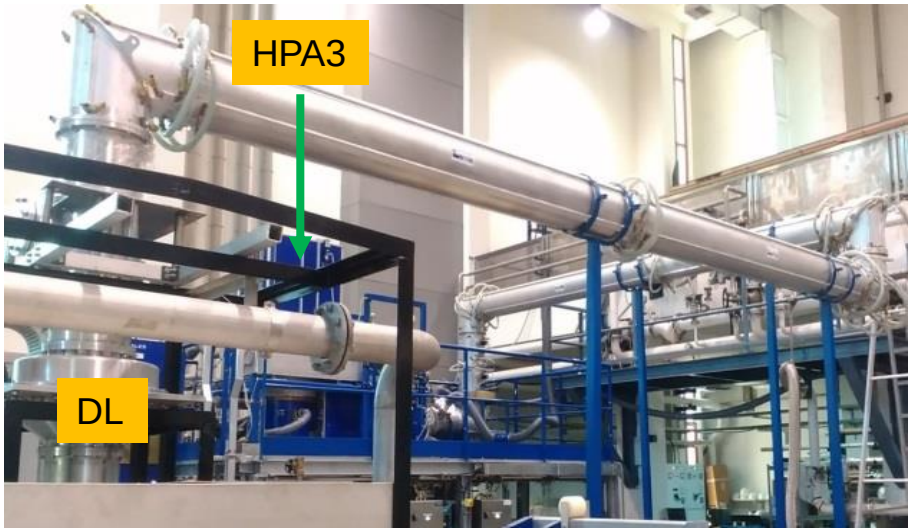
Mis-Match Tx-line (MMTL) system: Stub + Phase Shifter combination



Commissioning Results

HPA2 and HPA3 were assembled and integrated with auxiliaries & other sub-systems at Indian test facility





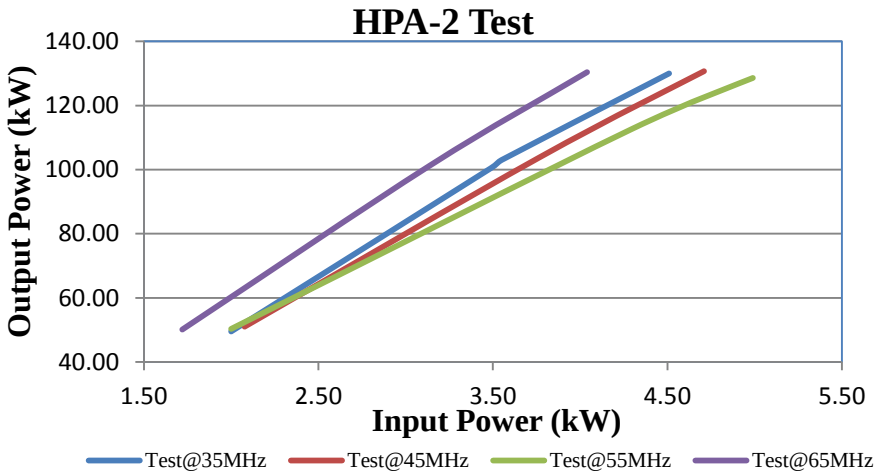
Prior to high power RF test, the system was subjected for

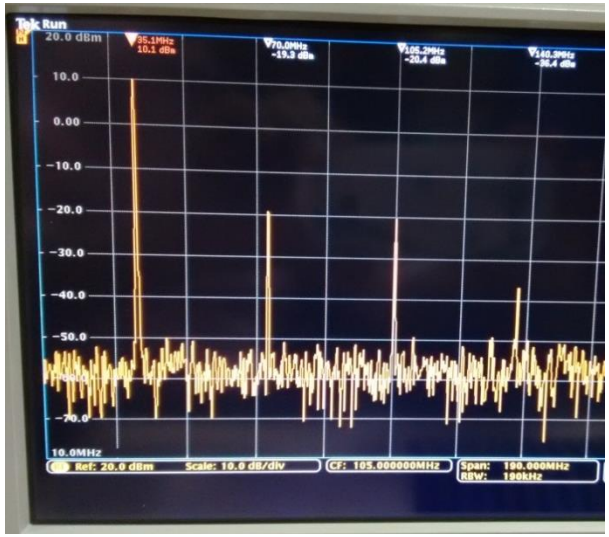
Tuning (within 180s)	±1MHz Bandwidth (BW) test	Higher Order Mode (HOM) test (without application of RF)
Operating frequency range 35-65 MHz	HVPS kept at 14.5kV/1A for HPA2 &16.5kV/5A for HPA3	HV kept at same level as BW test, however, Ia kept at 8A (HPA2)/40A (HPA3) by adjusting CGPS voltage

High Power RF Test – HPA2

Test Results of HPA2 on Matched Load (VSWR1:1)

Freq. (MHz)	P_{output} (kW)		V_{Anode} (kV)	I_{Anode} (A)	$Anode_{dis}$ (kW)	SG_{dis} (W)
	SSPA	HPA2	HPA2	HPA2	HPA2	HPA2
35	4.5	131.7	14.0	15.3	82.5	267.5
45	4.7	132.6	14.0	14.0	63.4	377.5
55	5.0	128.6	14.5	15.0	81.4	85.0
65	4.1	134.7	14.0	15.6	83.7	568.7



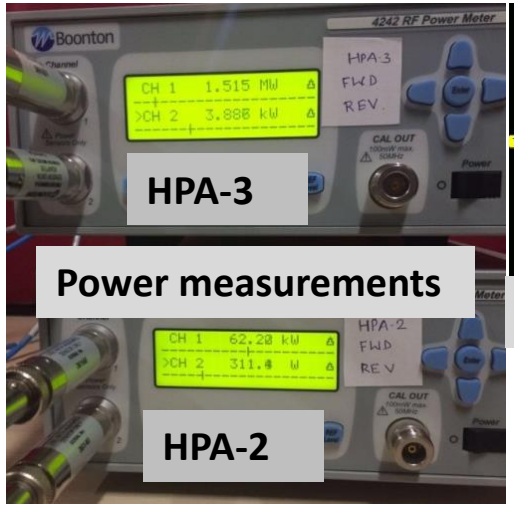


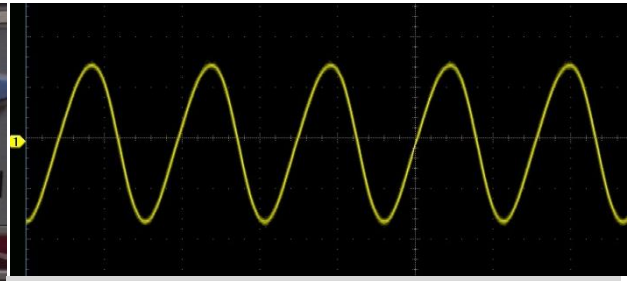
Harmonic level (35MHz/130kW):
ΔH1: -37.2dBc,
ΔH2: -43.7dBc,
ΔH3: -61.6dBc

High Power RF Test – HPA3

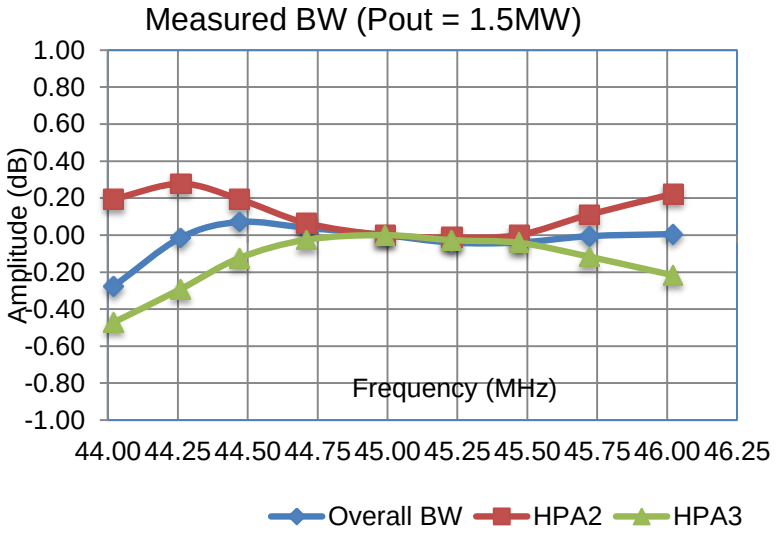
Test Results of Global Chain (SSPA + HPA2 + HPA3) on Matched Load

Freq. (MHz)	P_{output} (kW)			V_{Anode} (kV)		I_{Anode}(A)		$Anode_{dis}$(kW)	SG_{dis} (kW)
	SSPA	HPA2	HPA3	HPA2	HPA3	HPA2	HPA3	HPA3	HPA3
36	2.2	70.5	1705	14.5	23.0	9.9	128.5	1251	6.68
45	2.6	74.2	1526	14.0	20.0	11.2	123.8	950	6.53
55	2.2	58.2	1540	14.0	20.0	10.1	124.5	950	4.80
65	1.2	47.7	1503	14.0	20.0	8.4	115.4	805	4.34



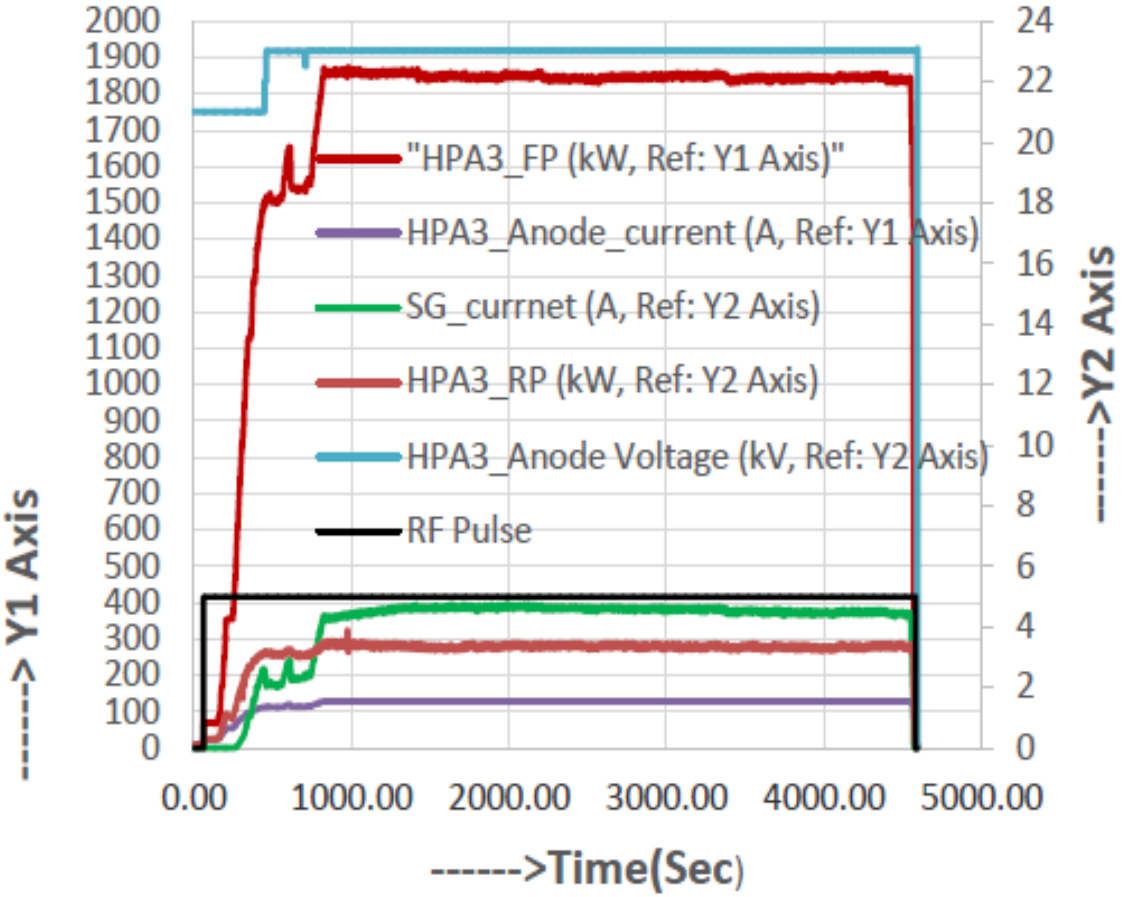


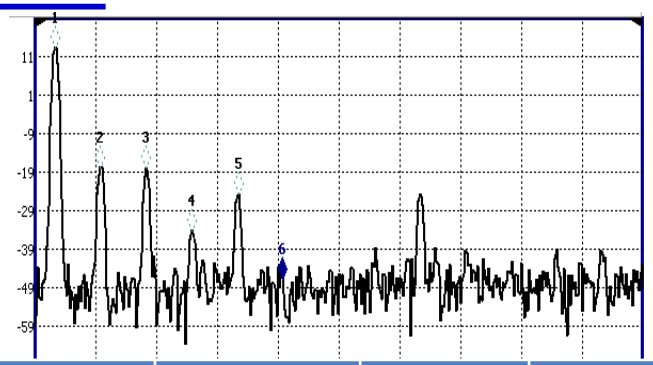
Oscillogram for forward power



Design Capability Test – HPA3

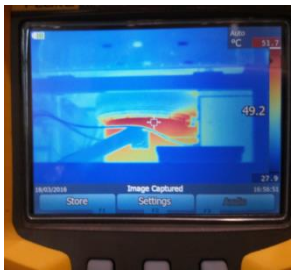
Run test on matched load: 1.7MW/36MHz/3600s





ΔH1 (dB)	ΔH2 (dB)	ΔH3 (dB)	ΔH4 (dB)
-37.51	-43.59	-61.87	-53.92

Monitoring of plate blocking capacitor temperature to define the duty cycle for heat run test



During power test ~ 60^0 C

After cool down ~ 1 Hr. ~ 32^0 C

High Power RF Test – HPA3

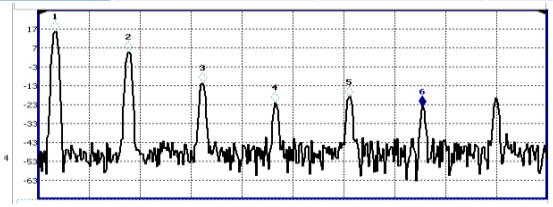
One of the important specifications: to demonstrate constant output power even with VSWR condition (up to 2:1) at any phase angle

Ensuring constant IC power to ELMy plasma

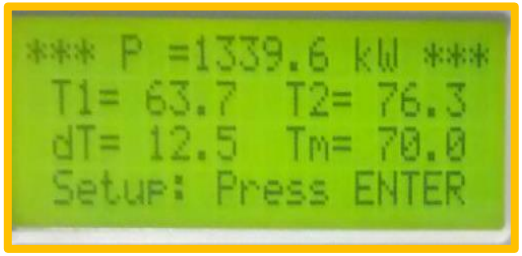
Test Results of Global Chain (SSPA + HPA2 + HPA3) on VSWR 2:1 at 65 MHz

Ref. angle (Deg.)	P_{output} (kW)			V_{Anode} (kV)		I_{Anode}(A)		$Anode_{dis}$ (kW)	SG_{dis} (kW)
	SSPA	HPA2	HPA3	HPA2	HPA3	HPA2	HPA3	HPA3	HPA3
0	1.0	28.9	1520	14.0	24.0	6.9	83.0	645.0	3.5
45	1.1	32.3	1501	14.0	25.0	7.2	85.6	806.3	2.3
90	1.4	47.5	1505	14.0	20.5	8.4	117.0	1067.5	6.3
135	1.9	72.0	1506	12.0	17.0	10.2	147.0	1159.3	5.5
180	2.2	87.7	1503	14.0	16.0	11.0	164.0	1281.8	6.3

ΔH1 (dB)	ΔH2 (dB)	ΔH3 (dB)	ΔH4 (dB)
-23.4	-42.1	-53.6	-51.0



Calorimetric measurements



Even with **11% power reflection** (corresponding to VSWR 2:1) forward power could be kept constant to **1.5MW**

High Power RF Test

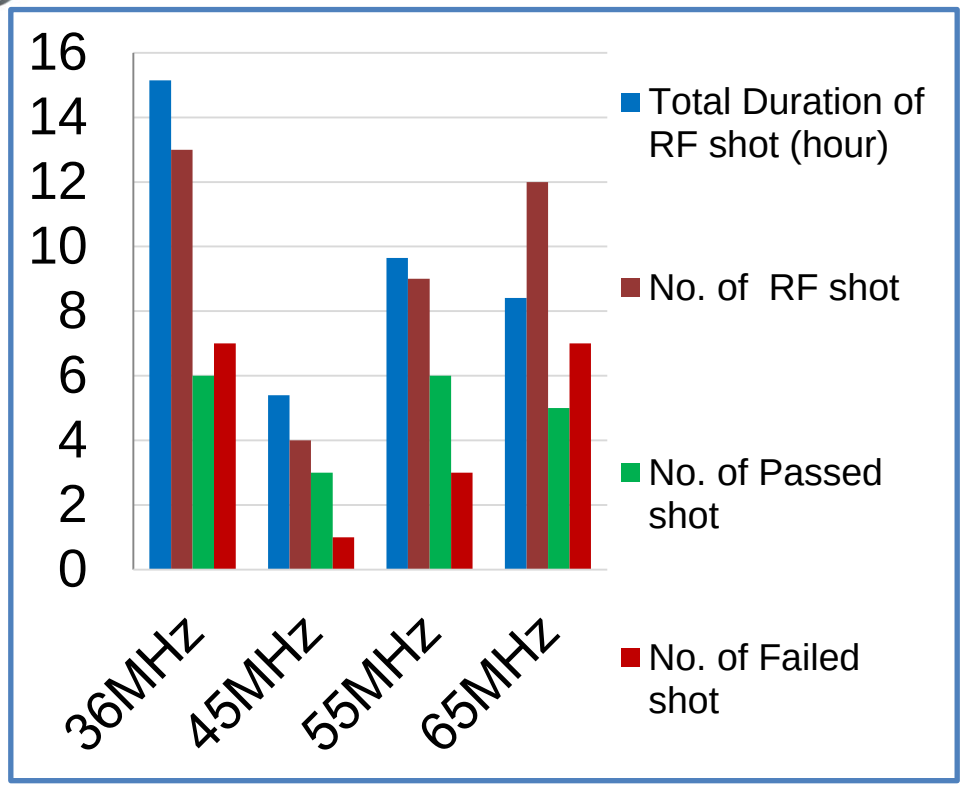
5 successive pulses tested with 25% duty cycle at 1.5 MW power level for 2000 s

- **On matched load**
- **On mismatched load**

Overall electrical efficiency : 55% - 65%
RF exposure limit: < 30 $\mu W/cm^2$

Modules	Designed Gain	Achieved Gain
SSPA	70dB	70dB
HPA-2 (TH781)	13.5dB	14-15dB
HPA-3 (TH628L)	12-15dB	12.7-14.8dB

Statistical analysis during initial RF operation



After performing all corrective actions, Burn test conducted for 6000s to verify the ruggedness of the entire system & benchmark the technology for fusion application

36MHz:
- HVPS trip (1 shot)
- HPA3 SG current is higher than expected value, hence terminated (3 shot)
- Difficulties in achieving BW (3 shots)

❑ **Corrective actions:**
- Proper tuning performed

45MHz:
- Over FP- during BW check at 1.5MW (1 shot)

❑ **Corrective actions:**
- Minor tuning performed.

55MHz:
- Higher Inlet temperature (1 shot)
- Over APD (1 shot)
- Anode OC (1 shot)

❑ **Corrective actions:**
- Minor tuning performed.

65MHz:
- Arcing in o/p transformer (1 shot)
- HVPS OV/ HP3 SG OC (4 shot)
- HVPS OC (2 shot)

❑ **Probable reason:** Arcing, component failure in SGPS

❑ **Corrective actions:** Replacement of components

Demonstrated Capability

R&D Specification	Diacrode based system
1.5MW / 2000s / 35-65 MHz / up to VSWR 2:1 with different phase angles	Demonstrated at 4 different frequencies
Design capability test at 1.7MW/3600s on matched load	Performed at 36 MHz & 65 MHz
η ~ 50% - 60%	55% - 65%
BW:±1MHz at 1dB	Successfully achieved
5 successive pulses at 1.5MW/2000s with 25% duty cycle	Demonstrated
Max. output harmonic level: < -20 dBc	Achieved
Emergency power cut-off response: <10 micro sec	Achieved
RF exposure limit: < 1.0 mW/cm2	< 30 μW/cm2

Summary

- Development of ITER R&D source using Diacrode tube is unique and first of its kind
- Burn test conducted for 6000s continuously to verify the ruggedness of the entire system and benchmark the technology for fusion application
- Data base generated is very useful information for future need in other scientific program
- Outcome of R&D phase will lead to establish the technology suitable for ITER & beyond ITER application

Thanks for your kind attention !

For more details please visit Poster Session FIP/1