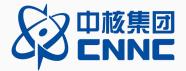


Validation and comparison of FPGA-based Real-Time Thomson Scattering data processing against offline analysis methods

Wenyan.Zhai,Zichen.He,Wenping.Guo,Shaobo.Gong, Chunhua.Liu,Zhipei.Hou,Junbin.Wu,Xing'an.Long, HL-3 Team Southwestern Institute of Physics (SWIP)





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- 02 Design Basis
- **103** Implementation Process
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- 05 Conclusion



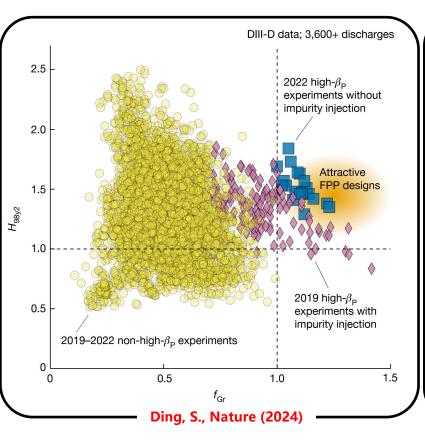


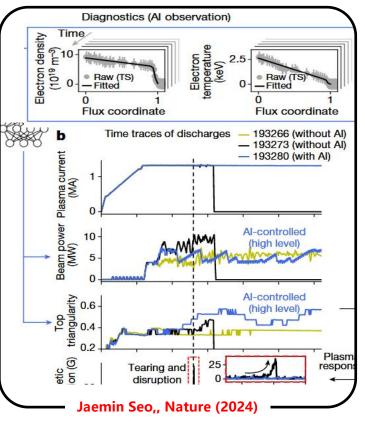
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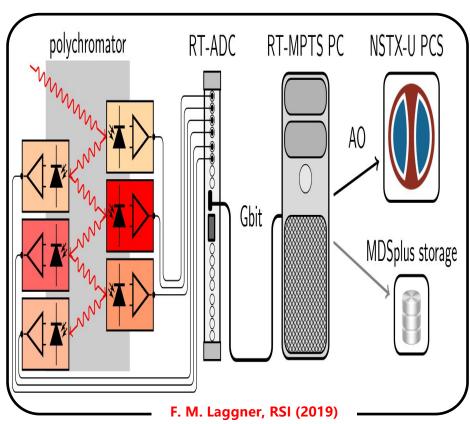
Background

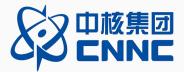


- Operate in high-density, high-confinement regimes;
- Advanced profile control needs real-time T_e and n_e;
- **Compute must beat millisecond-level GPU latency**;





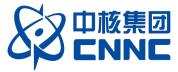




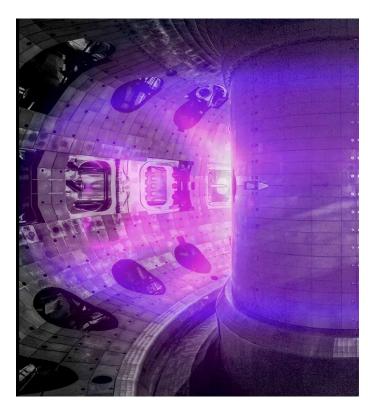


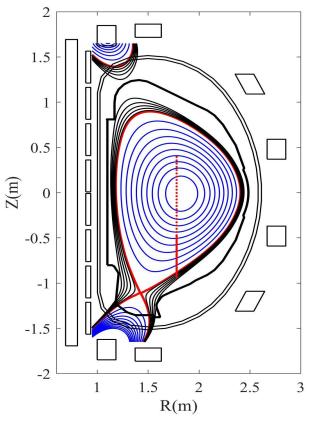
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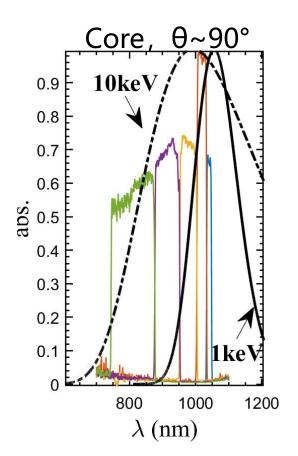
Design Basis

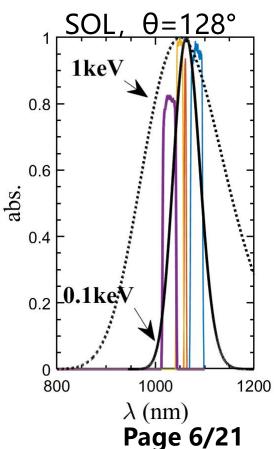


- On HL-3 in Spring 2025, the Thomson scattering system used a vertical laser beam with 60 spatial points
- Covering $T_e = 0.1-10$ keV and n_e of 5×10^{18} m⁻³— 2×10^{20} m⁻³;
- A 1064nm@2J Nd:YAG laser enabled 30 Hz temporal and 1–2 cm spatial resolution.





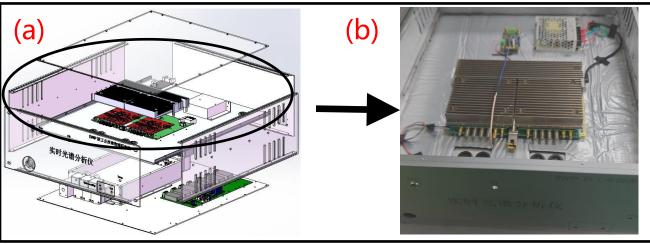


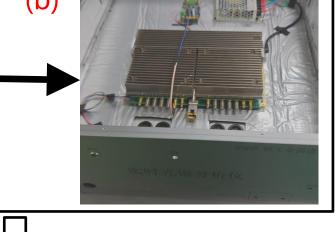


Design Basis

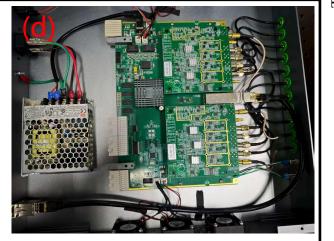


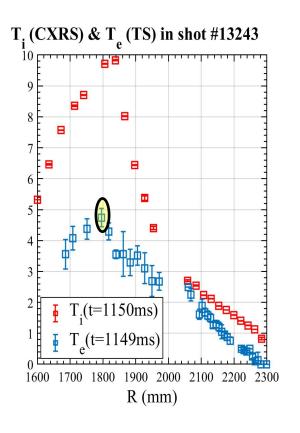
- RT-TS was developed and validated on the existing polychromator.
- Core spatial points were selected to support disruption prediction.

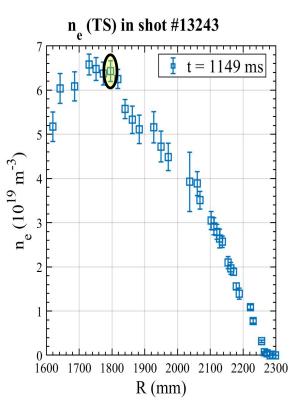
















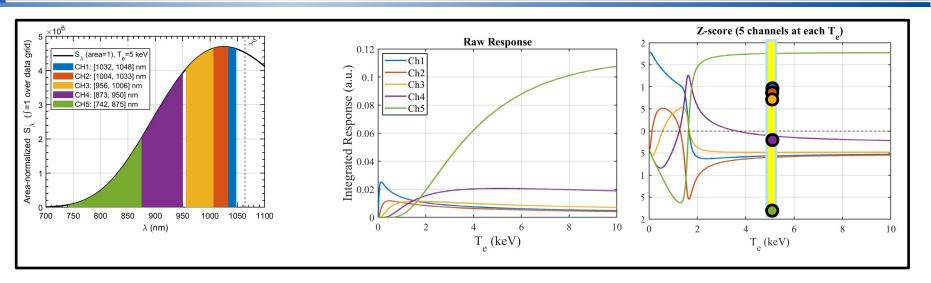
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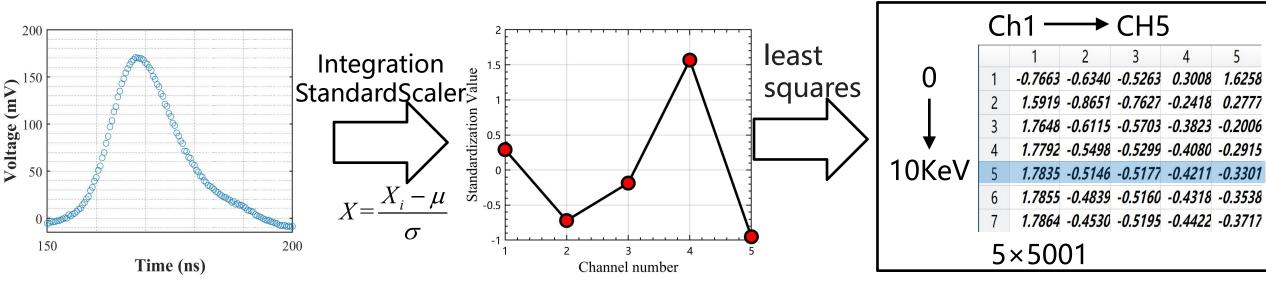
Implementation Process



Calculate Te

- Waveform Integration
- Integral Extraction
- Normalization
- Least-Squares Table Lookup

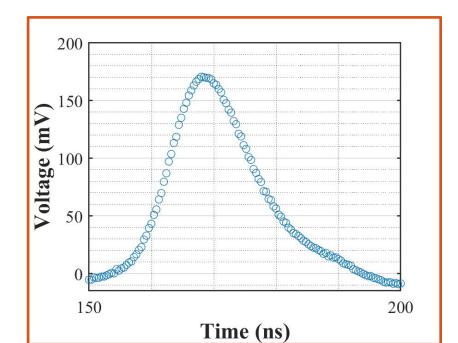


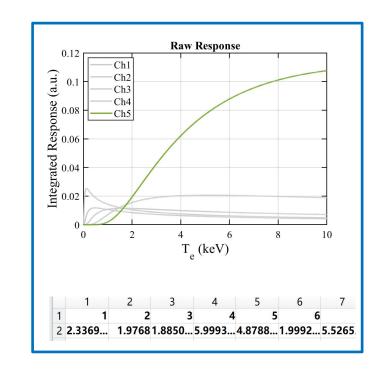


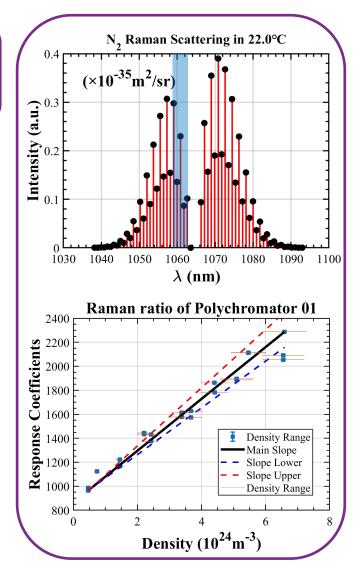
Implementation Process



$$n_{e,i} = S_{i,TS} \bullet (\frac{\sum \sigma_{Raman}(\lambda_i) \bullet R(\lambda_i)}{\sigma_{TS} \bullet \int f_{i,TS}(T_e) \bullet R(\lambda_i) d\lambda}) \bullet \frac{1}{\partial_i} = \frac{S_{i,TS}}{\int \int f_{i,TS}(T_e) \bullet R(\lambda_i) d\lambda} (\frac{\sum \sigma_{Raman}(\lambda_i) \bullet R(\lambda_i)}{\sigma_{TS} \bullet \partial_i})$$



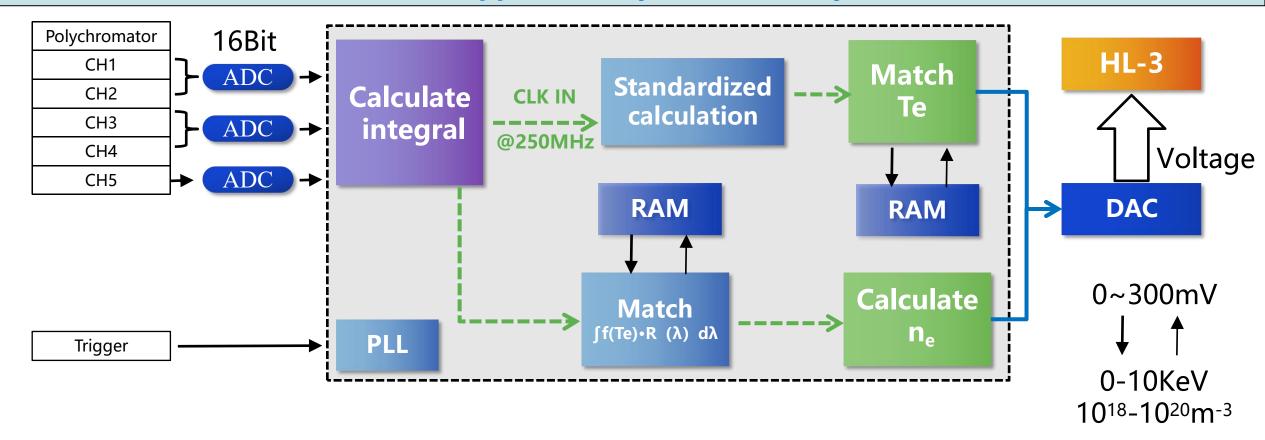




Implementation Process



- The acquired raw signals are baseline-subtracted before integration over the scattering time window.;
- The calculated T_e&n_e are then mapped linearly to the DAC by the FPGA.;





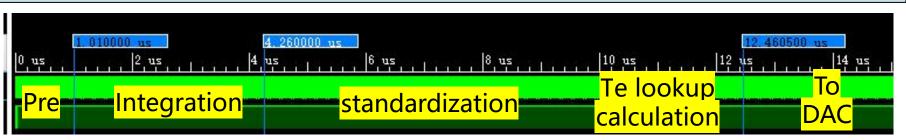


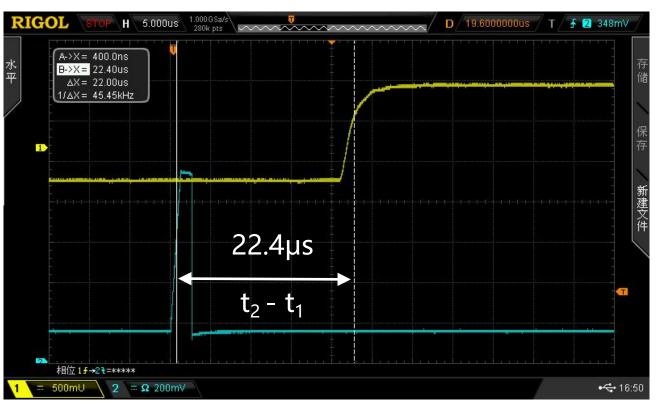
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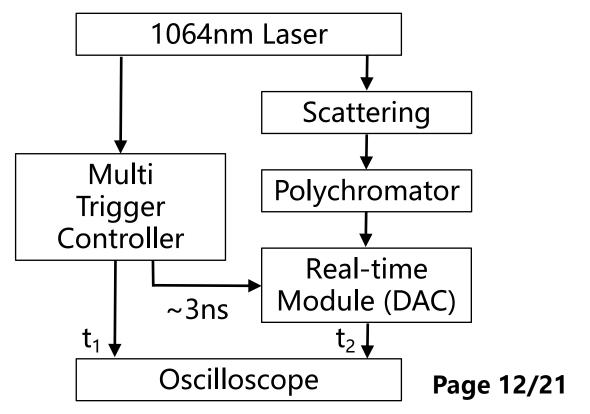


■ The simulated FPGA computation of T_e takes about 12.46 µs, while oscilloscope measurements show a trigger-to-result latency of about 22.4 µs.

Vivado2018 Simulating the computation takes time:

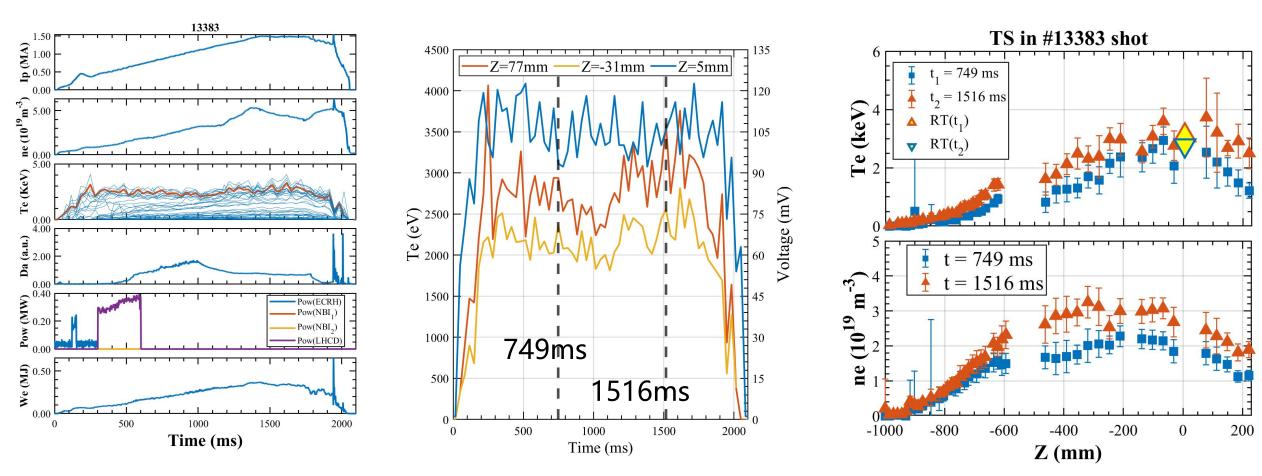








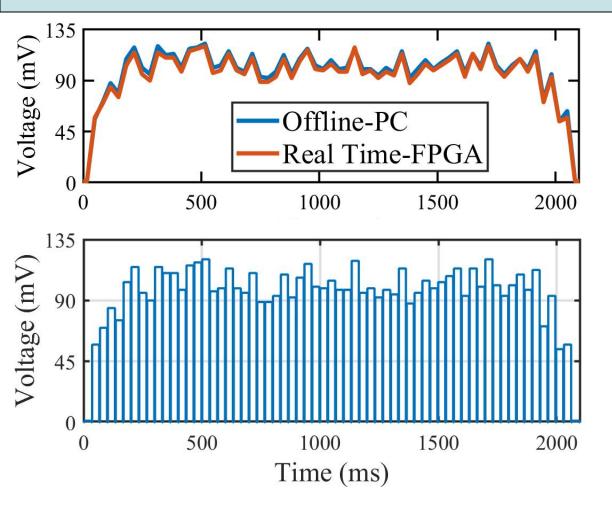
- The time evolution of T_e is consistent with that of neighboring channels.
- After conversion from mV to eV, the profile features are fairly consistent.

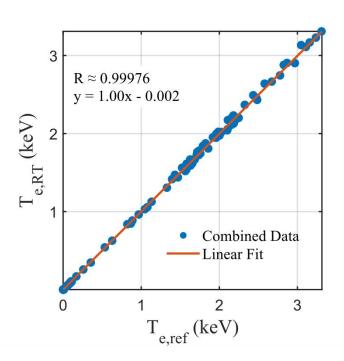


Note: Due to cable transmission constraints, only the real-time T_e results.



- The data recorded by the real-time module were recalculated on a Offline-PC, yielding results consistent with those from the FPGA.
- The real-time DAC outputs an analog signal, with each computed result held at a flat-top level for 30 ms.





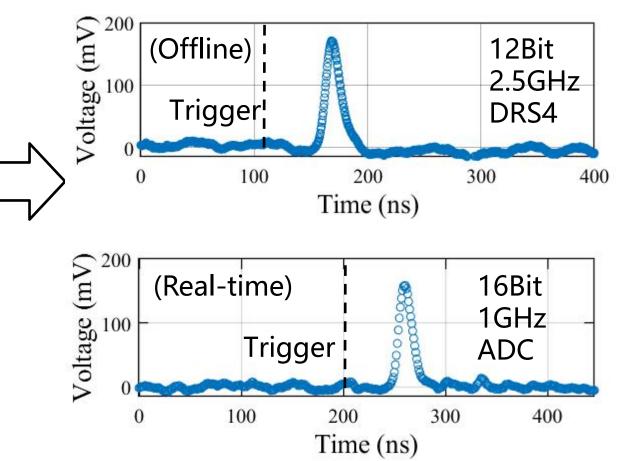
Note: The DAC voltage output is affected by environmental noise.



- The calculation accuracy is mainly determined by the fidelity of the raw signals.
- The polychromator output ranges from 0 to 500 mV with a pulse width of ~20 ns.
- Under the same noise conditions, ACQ of real-time module provides superior performance.



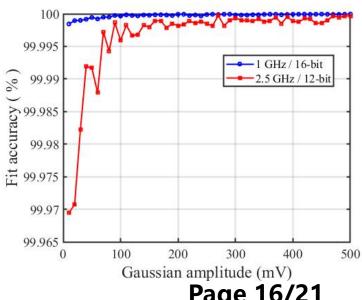
0-500mV FWHM~20ns



$$y_{true}(t) = A_0 \exp\left[-\frac{(t - t_0)^2}{2\sigma^2}\right]$$

$$NRMSE = \frac{\sqrt{\frac{1}{N}\sum_{k} (y_{fit}(t_k) - y_{true}(t_k))^2}}{A_0}$$

$$Fit _Accurary(\%) = 100 \times (1 - NRMSE)$$



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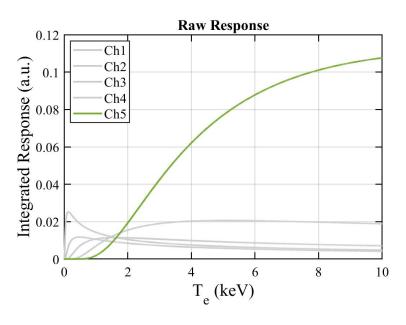


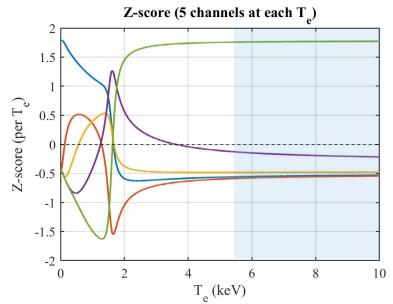
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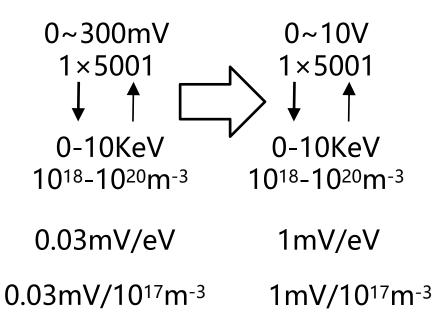
Limitations



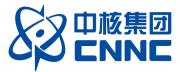
- One channel used for density evaluation are not suitable for the table-lookup method.
- With the 5-channel polychromator, lookup bias becomes significant for Te~10KeV;
- A higher-precision DAC is needed, with output range extended to 10 V.



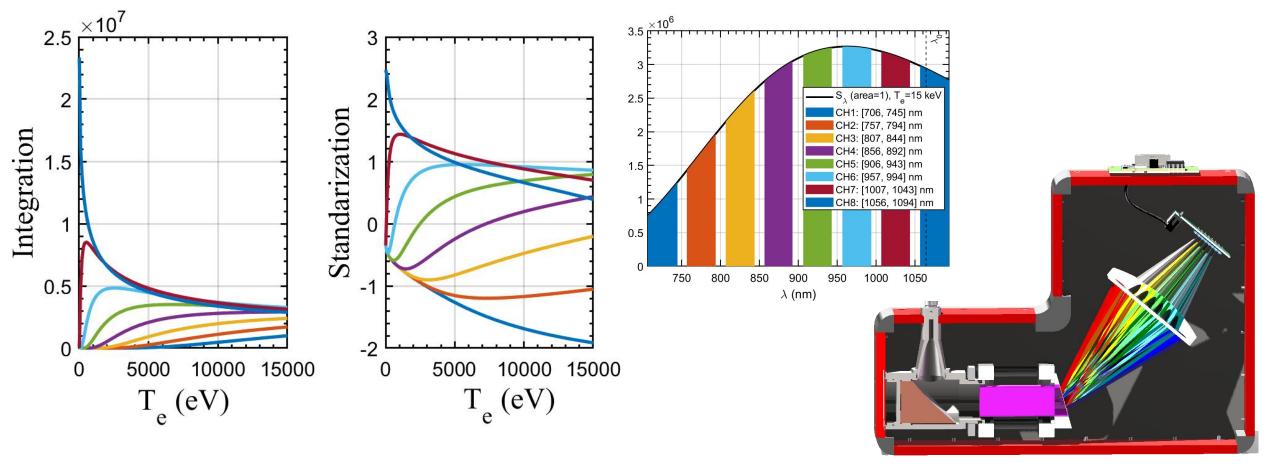




Development Plan

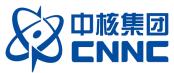


- To access higher HL-3 operating regimes (10–15 keV), develop an 8-channel polychromator.
- For density lookup, add a spare channel and select computation based on SNR or validity range.



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Summary And Outlook



Summary

- 1. Real-time T_e computation was developed and validated at a single spatial point.
- 2. The real-time processing runs on a FPGA;
- 3. software emulation shows a T_e compute time of ~12.4 µs, and the instrument's trigger-to-TTL output latency is ~22.4 µs.
- 4. The real-time results track the experimental $T_{\rm e}$ evolution, and raw data acquired during real-time operation, when recomputed offline, achieve a 99.91% correlation with the FPGA outputs.

Outlook

- 1. To improve output accuracy, a higher-precision DAC with an extended 10 V range is required.
- 2. To enhance core T_e accuracy on HL-3, an 8-channel polychromator optimized for the 10–15 keV range should be developed.
- 3. For robust n_e evaluation, multiple channels should be incorporated into the computation.



Thanks

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