CONFERENCE PRE-PRINT

OVERALL PERFORMANCE OF THE HOUR-LEVEL ALTERNATING HYBRID INTEGRATOR

One of the key instruments for long-term magnetic diagnostic systems

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Abstract

This paper introduces an alternating integration system that employs dual-parallel integrators. The system incorporates phase-locked reset cycles and adaptive digital compensation: a real-time acquisition algorithm continuously identifies and calibrates the drift curve of each integrator unit, while a τ-calibration algorithm dynamically matches their time constants to within 0.05 %. Bench test data show that the integrator drift remains at 0.1 % full-scale range (FSR) over a 4000s interval, with a 3σ dispersion below 17 mV and the mean integration output approximated the ideal 0 V reference. During the EAST's 2024 winter plasma discharge campaign, the optimized integrator exhibited a drift of only 9 mV after a 1066 s discharge—more than an order-of-magnitude improvement over legacy units and fully compliant with current experimental requirements. While meeting all accuracy specifications, the single-channel cost is only 3000–4000 RMB—roughly one-half to one-third of the price of the F4E prototype for ITER. These advances not only satisfy EAST's stringent 1000s discharge requirement but also furnish a production-ready, high-performance, and cost-effective option for ITER and the forthcoming BEST program.

1. INTRODUCTION

In January of this year, the Experimental Advanced Superconducting Tokamak (EAST) achieved a high-performance plasma discharge lasting 1066 seconds, approaching its maximum design target. During this milestone, the electromagnetic diagnostic system (EDS) —comprising more than 600 measurement channels – played a critical role in monitoring and controlling plasma position, shape, and equilibrium configurations [1].

As a key component of the electromagnetic measurement system, the integrator is indispensable in determining fundamental plasma-diagnostic parameters [2]. Existing integrators, however, still face a fundamental challenge: its input errors accumulate over time, which becomes the primary factor degrading measurement accuracy as integration duration increases. To achieve precise magnetic measurements at the kilo second timescale, EAST requires the integrator's total error to remain below 0.1% of the full-scale range (FSR, ~20 mV). This translates to maintaining an average input-referred error at the nanovolt (nV) level when accounting for all error sources – an exceptionally demanding engineering task. This challenge is not unique to EAST but is also encountered in long-pulse tokamak facilities worldwide, including Korea Superconducting Tokamak Advanced Research (KSTAR), ITER, and the under-construction Burning Experimental Superconducting Tokamak (BEST) [4]. To address this, various facilities have developed different types of long-pulse integrators tailored to their specific needs, including analog, digital, and hybrid analog-digital designs. In addition, the large number of integrators required in a tokamak makes stringent cost control imperative. To meet these challenges, numerous integrator designs have been proposed [5], encompassing analog, digital, and hybrid analog-digital architectures. Among

publicly reported results, F4E's fully digital integrator, originally designed for ITER's requirements, has demonstrated the best benchtop performance to date [17]. Tests indicate it meets ITER's stringent 500 μV·s / hour precision requirement in theoretical estimations. However, this solution suffers from several limitations including high sensitivity to thermal noise, complex architecture, and high costs, making it less suitable for large-scale deployment.

This paper presents a novel hybrid alternating integrator design that employs two analog integrators to alternately perform real-time integration of input signals. The digital component learns and compensates for integration errors in real-time to enhance accuracy, effectively addressing issues inherent to analog integrators such as integration drift, circuit saturation, and nonlinear errors. The self-learning capability eliminates the need for the tedious tuning typically required by analog integrators, while maintaining a simple and robust architecture. Recent experimental results from EAST 2024 winter plasma discharge campaign demonstrate that its real-time compensated drift remains below 0.1 % of FSR for 1066 s, with peak drift less than 9 mV — an order-of-magnitude improvement over conventional integrators, which typically exhibit more than 1 % FSR drift. Extended 4000 s bench tests confirm compliance with EAST's hour-long discharge requirements and surpass the performance of F4E prototype for ITER, even in bench tests lasting up to 24 h, the drift remained within 200 mV, underscoring the system's superior performance. In addition, the single-channel cost is only 3000 – 4000 RMB, providing substantial economies of scale compare to the F4E prototype (> 8000 RMB per channel). The architectural details of integrators and optimization algorithm have been disseminated through peer-reviewed publications and protected via patent filings; moreover, a comprehensive manuscript that rigorously analyses its performance metrics and error theory is presently under editorial review.

This paper is organized as follows: Section 2 describes the system architecture, Section 3 presents the concrete experimental results of both bench test and field test, and Section 4 concludes with a discussion of the findings and future research directions.

2. STRUCTURAL OVERVIEW OF THE DRIFT-COMPENSATED DUAL-PARALLEL INTEGRATOR

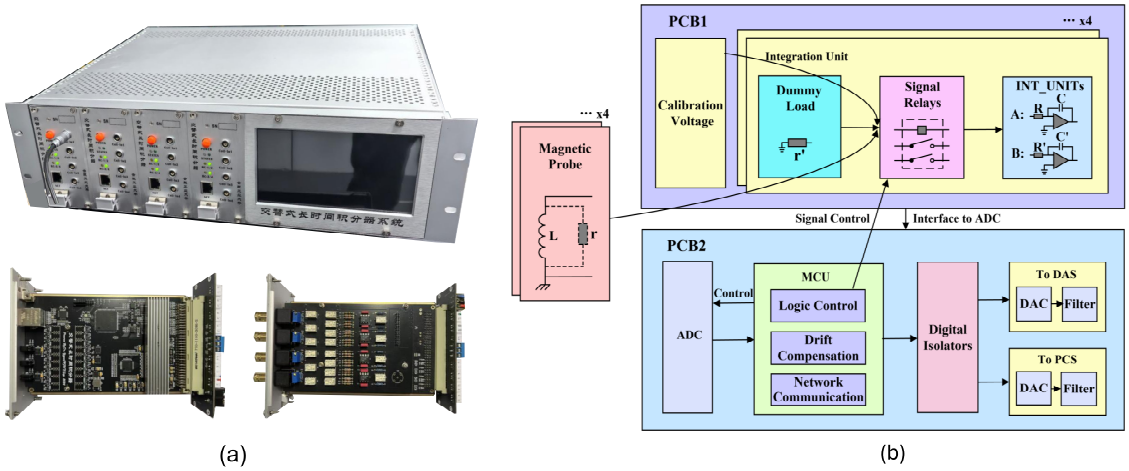

Fig. 1 Topology of the dual-INT_UNIT alternating integrator with dynamic drift compensation.

Fig. 1(a) shows the optimized integrator system, and its topology is illustrated in Fig. 1(b). A dual-parallel integrator operates alternately to avert saturation. Relay array enables real-time switching among different operating states of integrators. An MCU characterizes drift, extracts correction-algorithm parameters, applies real-time error compensation, concatenates the alternating integration results, and controls the relays in each signal path. The compensated data are then fed to a high-resolution DAC, which reconverts them to an analog signal for the data collection system (DCS) and the plasma control system (PCS). A digital isolator decouples the DAC from the preceding circuitry, preserving signal integrity, and each DAC channel is driven independently so that the output amplitude can be trimmed by adjusting the post-gain stage. Fig. 2 shows timing sequence of the calibration cycle. At any moment, only one integrator is engaged in probe signal integration. During the initial phase, INT_UNIT-A integrates the magnetic probe signal, while INT_UNIT-B is reset and subsequently connected to ground via a dummy load to characterize its drift characteristics. In the following phase, the operational roles of the INT_UNITs are interchanged: INT_UNIT-B performs probe signal integration while applying drift correction

based on its previously acquired drift profile, thereby yielding a net integration result. The microcontroller unit (MCU) subsequently concatenates the outputs from both INT_UNITs, producing a continuous, drift-compensated signal for downstream applications.

To maintain the integration consistency, a τ-calibration algorithm is also employed. Both INT_UNITs integrate an identical calibration voltage for the same time interval, so the ratio of their raw integration increments equals the ratio of their time constants (τ). The digital normalization approach largely eliminates hardware discrepancies between the two integrators, thereby significantly enhancing integration accuracy.

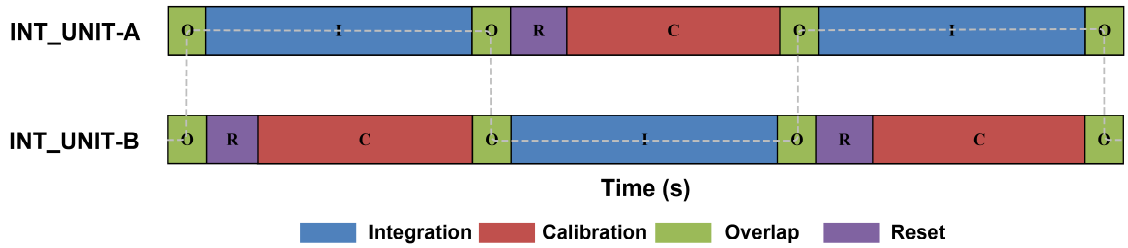

Fig. 2 Timing sequence of INT_UNITs alternating operation.

The input–output characteristics of the integrator's integration unit, digital front-end, and ADC are shown in Fig. 3, illustrating the end-to-end performance of the system's signal chain. As shown in Fig. 3(a), when an 8 Hz sinusoidal signal with a peak-to-peak amplitude of 18 V was applied to the integration system, the output waveform and amplitude matched the input, exhibiting a 90° phase lag. Under step-signal excitation Fig. 3(b), the output delay was less than 1 ms, meeting the system's response-speed requirements.

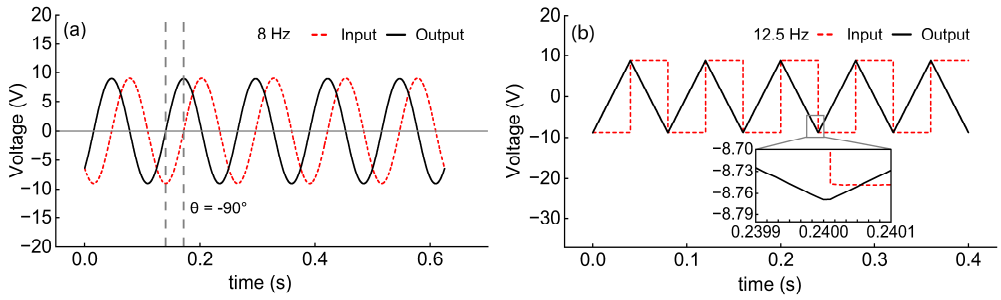

Fig. 3 input–output characteristics. (a) 8 Hz sine wave integration. (b) < 1 ms step response delay.

3. LONG-DURATION INTEGRATION PERFORMANCE TEST ON DIFFERENT SITUATION

3.1. Long-duration bench test

A long duration integration bench test was conducted to evaluate the baseline performance of the optimized integrator. Four integrators (integrator1-integrator4) were used for test, carried a total of 104 rounds, each lasting more than 4000 s. The corresponding drift characteristic are plotted in Fig. 4(a). Observation of the compensated drift distribution reveals a pronounced concentration, with the accumulated integration drift over 4000 s remaining below 600 μV·s, demonstrating the system's robust stability. For a direct comparison with the F4E prototype for ITER, the drift at the 2500s mark was recorded. The optimized integrator achieved 100 % compliance with the 500 μV·s / hour specification, whereas the F4E prototype exceeded this limit in 2.8 % of the tests. The drift distribution of 4000s for all channels is shown in Fig. 4(b). About 99.1% of the tests maintained integration drift within the 0.1 % FSR (20 mV) specification. Moreover, the drift exhibited a standard deviation and mean square error of 5.58 mV, while the mean integration output approximated the ideal 0 V reference within measurement uncertainty, demonstrating a high degree of performance consistency.

We also evaluated the drift distribution of different durations. The results are summarized in TABLE 1, demonstrate close alignment between theoretical analysis and experimental results, fully satisfy the EAST specification. Fig. 4(c) presents a comparison of the 1000 s drift nonlinearity between the optimized integrator and existing integrators. The existing units (PCBPV16T, PCBPL3T, PCBPL8T, and PCBPV11T) — even after drift compensation and τ-constant normalization — still exhibited significant nonlinear error (> 0.08 % FSR), whereas the optimized integrator reduced this error to below detectable levels (< 10 ppm). These data attest to the superior stability and suitability for ITER's integrator specifications.

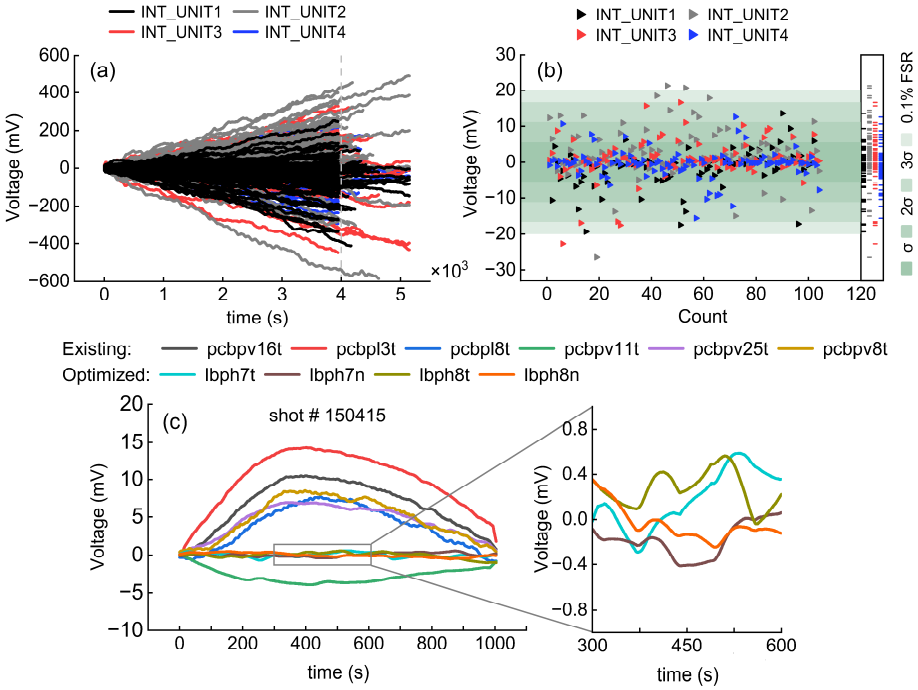

Fig. 4 Error dispersion characterization with nonlinearity validation and drift over 4000-second extended duration. (a) Integration drift characterization over 4000-second. (b) Error dispersion characterization of 416 test cycles. (c) Nonlinear drift of conventional integrators and proposed system.

TABLE 1. INTEGRATION DRIFT DISPERSION STATISTICS

Duration(s)	1σ	2σ	3σ	0.1%FSR	500 μV·s/hour
1000	98.80%	100.00%	100.00%	100.00%	100%
2000	89.66%	99.52%	100.00%	100.00%	100%
2500	87.02%	99.04%	99.76%	100.00%	100%
3000	84.38%	96.39%	99.52%	99.76%	100%
4000	79.33%	92.79%	97.36%	99.04%	99.76%

3.2. Field test of optimized integration system on EAST tokamak's plasma discharge campaign

3.2.1. Kilo-second-Scale Discharge Testing

During the EAST tokamak's 2024 winter plasma discharge campaign, a complete set of four alternating continuous integration system boards (totaling 16 channels) was deployed. Four channels—LBPH7T, LBPH7N, LBPH8T, and LBPH8N—were dedicated to discharge tests. They were installed at positions symmetric to the corresponding HBPH-prefixed channels—HBPH7T, HBPH7N, HBPH8T, and HBPH8N, enabling cross-validation between the two sets. The system began recording data on 11 December 2024, starting with shot #120115. Taking shot #150425 as a representative case, all four channels exhibited excellent performance: after a 1066s discharge, the integration drift in each channel remained below 9 mV, whereas existing integrators recorded drifts exceeding 100 mV—corresponding to an accuracy improvement of roughly 20 dB. The worst-case diagnostic accuracy, ΔB/B, is defined as the ratio of the maximum output voltage Vmax (corresponding to the peak magnetic field B) to the instantaneous integration drift ΔV (derived from linear drift, equivalent to ΔB). The

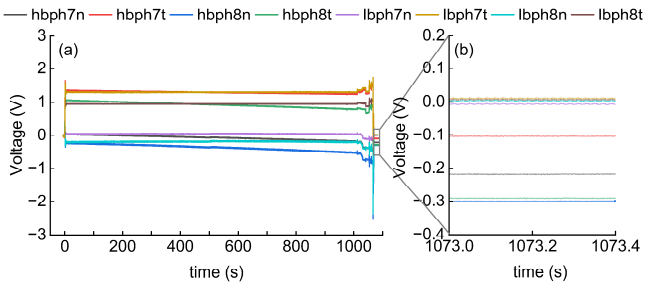

Fig. 5. EAST 1066-second discharge performance. (a)Integration results at each position of shot #150425. (b) Integration drifts after EAST 1066-second discharge.

optimized integrator complies fully with the 1 % specification, whereas existing integrators exceed the allowable control-accuracy limits, as summarized in TABLE 2 and illustrated in Fig. 5. Taken together with the other test results, these data confirm that the alternating, continuous-integration architecture satisfies the performance requirements for 1 000-s discharges on the EAST tokamak.

TABLE 2. COMPARATIVE INTEGRATION DRIFT PERFORMANCE DURING EAST 1066-SECOND DISCHARGE

Signal	drift voltage magnitude (mV/V•s)	Magnetic field variation period (ΔB/B)
HBPH7T	$103.97/2.08\times10^{-3}$	5.44%
HBPH7N	$219.71/4.39\times10^{-3}$	19.04%
HBPH8T	$291.26/5.83\times10^{-3}$	14.70%
HBPH8N	$300.62/6.01\times10^{-3}$	13.02%
LBPH7T	$8.98/1.87\times10^{-4}$	0.67%
LBPH7N	$5.54/1.15\times10^{-4}$	0.85%
LBPH8T	$5.96/1.24\times10^{-4}$	0.26%
LBPH8N	$6.70/1.39\times10^{-4}$	0.19%

3.2.2. 24-hour multiple continuous short-term discharges pulse drift testing

The forthcoming BEST tokamak is intended to deliver the world's first on-grid demonstration of fusion power, providing a significant advance in burning-plasma physics and an essential step in China's fusion-energy roadmap. Pulse durations are exceeding one hour and, ultimately, to approach day scale—regimes for which existing integrators are manifestly inadequate. Accordingly, ultra-long integration tests were carried out to quantify the performance and furnish empirical data for subsequent design refinements. Because of constraints in the EAST discharge schedule and the substantial duration required for each test, only some limited set of 24 h bench tests could be completed. As summarized in Fig. 6, the 24 h accumulated drift of a single channel remained below 200 mV in four independent tests. It indirectly reflecting the superior long-term stability of the optimized integrator.

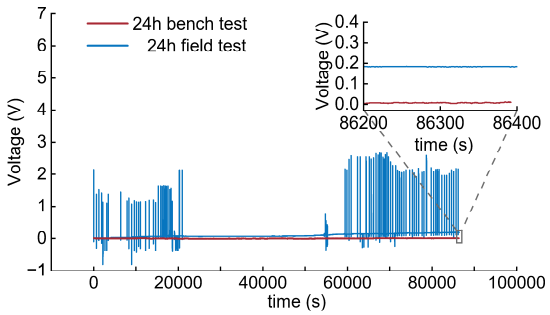

Fig. 6. Multi-pulse drift test over 24-h extended duration.

4. CONCLUSIONS

Developing integrators that can constrain drift to specified limits over kilo-second and even hour-scale intervals is essential for maintaining plasma stability during tokamak operation. This paper proposes an alternating integration system based on dual parallel integrators. By uniting the real-time integration capability of analog integrators with the flexibility of digital drift compensation, the design achieves long-duration, high-precision performance within a simple structure. The cost per channel is roughly 1/2 to 1/3 of that of the F4E prototype for ITER, making the system particularly attractive for large-scale deployment. Moreover, the input impedance has been increased to above 200 kΩ, fully meeting the requirements of both BEST and ITER. Compared with digital integrators, the design is virtually unaffected by thermal noise. Comprehensive bench and field tests confirm its superior performance: the optimized integrator fully meets EAST's kilo-second-level discharge requirements and provides a robust technological foundation for the electromagnetic diagnostic system of the forthcoming BEST tokamak.

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