OVERALL PERFORMANCE OF THE HOUR-LEVEL ALTERNATING HYBRID INTEGRATOR

One of the key instruments for long-term magnetic diagnostic systems

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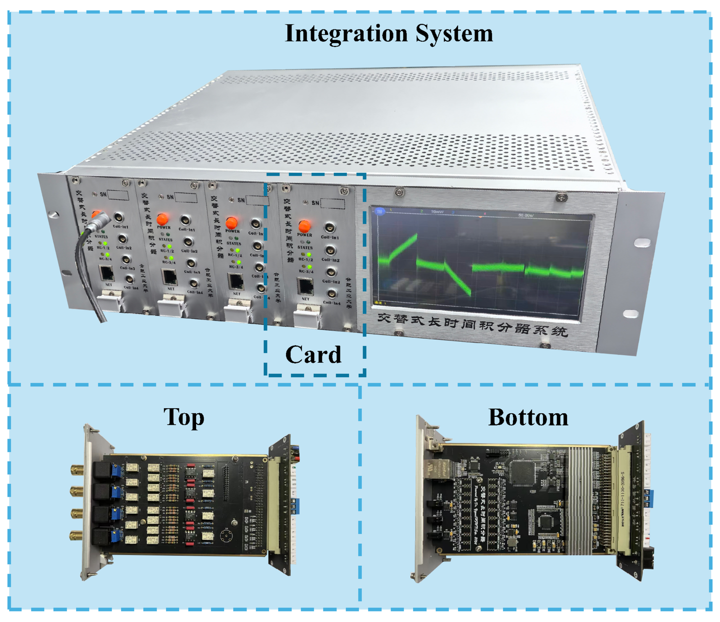
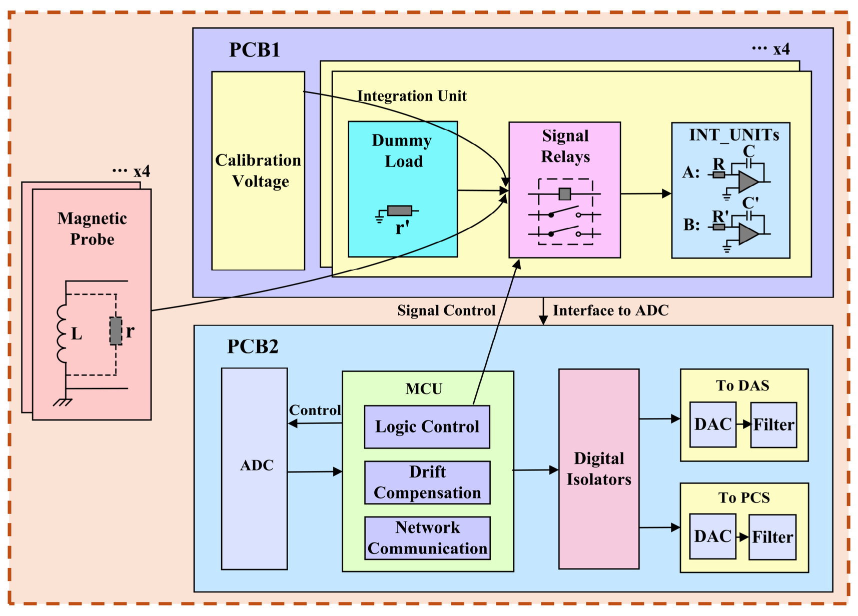
Introduction

As of January 2025, EAST has achieved a record 1066-second high-performance plasma discharge, wherein the electromagnetic diagnostic system (EDS) with over 600 channels played a vital role. However, the prevailing integrators, plagued by inherent drift, nonlinear errors, and circuit saturation, have emerged as a critical bottleneck constraining further extension of discharge duration. To address this, we present a novel hour-level alternating hybrid integrator. This architecture employs dual analog integrators operating alternately, where the inactive unit is reset to prevent saturation, enabling continuous long-pulse measurement. It strategically maintains low terminal voltage on integration capacitors to mitigate leakage current-induced nonlinear errors and incorporates a self-learning mechanism for adaptive digital compensation of intrinsic drift. Furthermore, through time-constant calibration and normalization, the system ensures unbiased stitching of outputs from both integrators, while data-driven optimization of operational parameters minimizes error dispersion across the system. Bench tests demonstrate a drift of less than 0.1% FSR over 4000 seconds, and field results on EAST confirm a mere 9 mV drift after the 1066-second discharge — an order-of-magnitude improvement over legacy units — all achieved at a production-ready, cost-effective level suitable for large-scale deployment.

Structure





Multi-channel design.
Four channels per board.
Up to four boards integrated per chassis.

Dual-integrator architecture.
Alternating operation enables continuous integration and saturation suppression.

High-precision ADC/DAC & High-speed MCU.
Ensures accurate signal conversion and reconstruction.
Enable millisecond-level response for real-time drift compensation and relay control.

Digital isolation & Filtering.
Maintains signal integrity and suppresses interference, ensuring reliable analog outputs for the DCS and PCS.

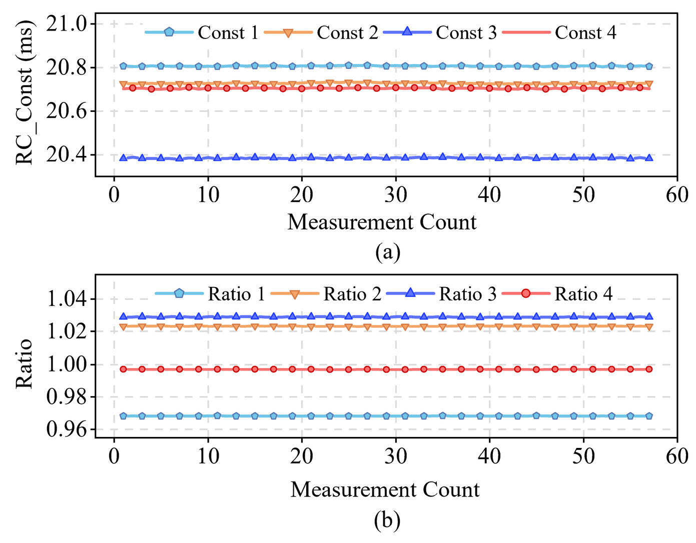
Methods

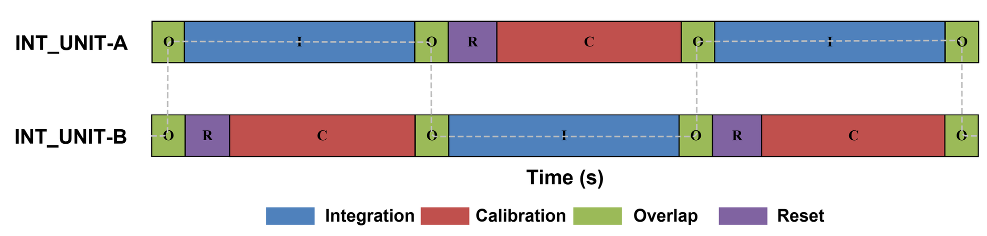
τ calibration mechanism .
A τ-calibration mechanism and digital normalization process ensure unbiased stitching of the output signals from the alternating integrator pairs, guaranteeing continuous and accurate integration.

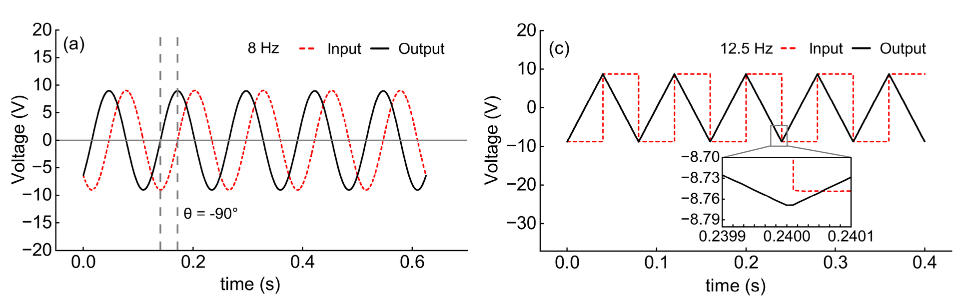
adaptive digital compensation.
Based on cycle-based drift learning and adaptive digital compensation, each integrator autonomously corrects its errors. This significantly improves accuracy, reduces dependency on component precision and integrator symmetry, and eliminates manual calibration, facilitating mass production and deployment.

high real-time performance.
The proposed hybrid architecture achieves continuous, drift-compensated integration with millisecond-level response.

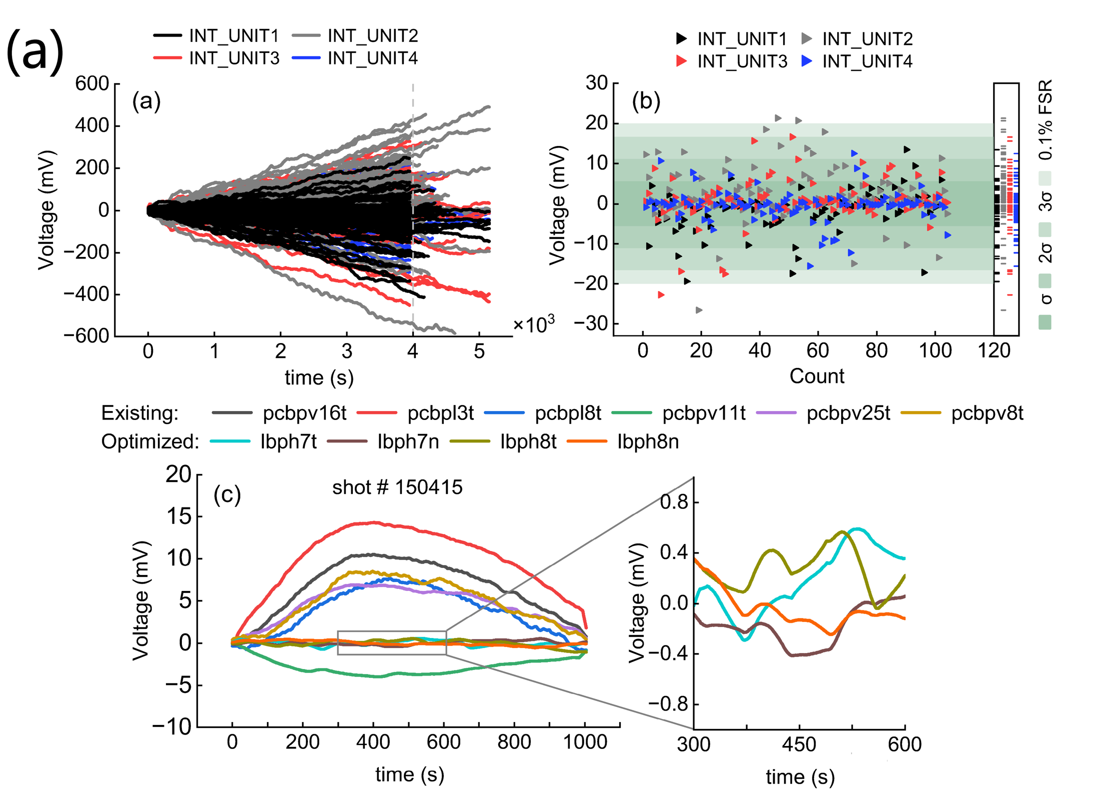
(1) $RC = \frac{V_{REF} \times \Delta t}{V}$ (2) $RC_B = \frac{\Delta V_A \times RC_A}{\Delta V_B}$







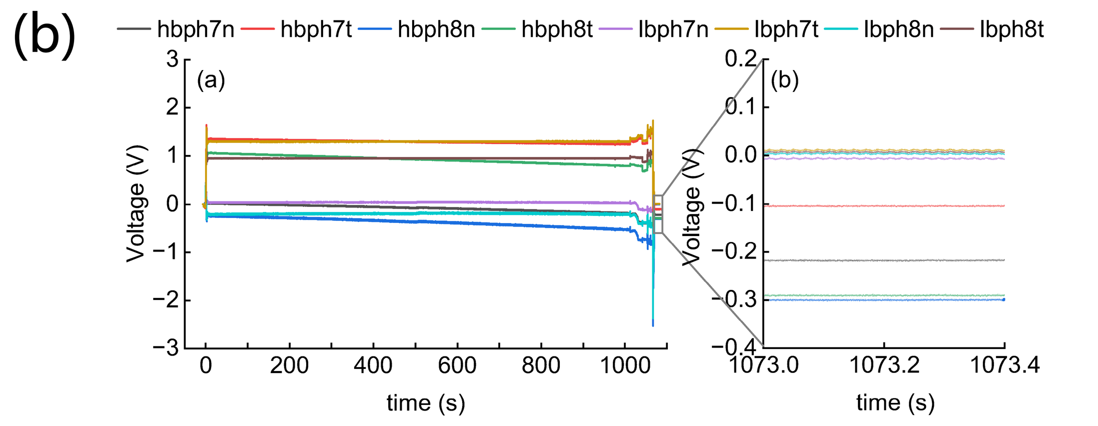
Bench and Field Tests



INTEGRATION DRIFT DISPERSION STATISTICS

Duration(s)	1σ	2σ	3σ	0.1%FSR	500 μV·s/hour
1000	98.80%	100.00%	100.00%	100.00%	100%
2000	89.66%	99.52%	100.00%	100.00%	100%
2500	87.02%	99.04%	99.76%	100.00%	100%
3000	84.38%	96.39%	99.52%	99.76%	100%
4000	79.33%	92.79%	97.36%	99.04%	99.76%

(a) Long-duration bench test
4000s continuous operation with drift < 0.1 % FSR (3σ < 17 mV);
output remained near 0 V, confirming excellent thermal stability.

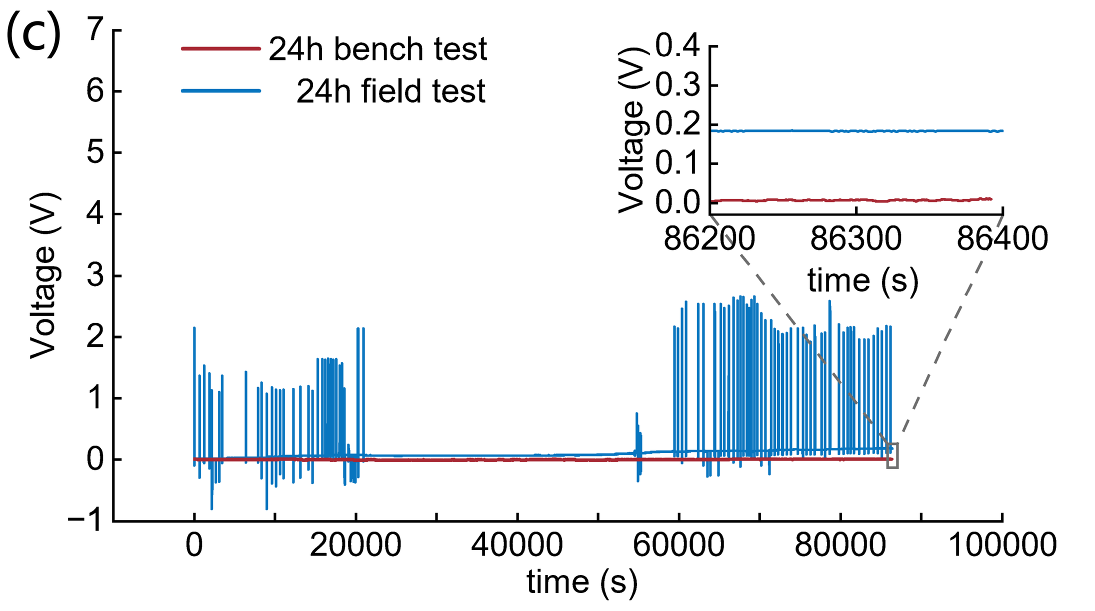


COMPARATIVE INTEGRATION DRIFT PERFORMANCE DURING EAST 1066-SECOND DISCHARGE

Signal	drift voltage magnitude (mV/V•s)	Magnetic field variation period (ΔB/B)
HBPH7T	$103.97/2.08\times10^{-3}$	5.44%
HBPH7N	$219.71/4.39\times10^{-3}$	19.04%
HBPH8T	$291.26/5.83\times10^{-3}$	14.70%
HBPH8N	$300.62/6.01\times10^{-3}$	13.02%
LBPH7T	$8.98/1.87\times10^{-4}$	0.67%
LBPH7N	$5.54/1.15\times10^{-4}$	0.85%
LBPH8T	$5.96/1.24\times10^{-4}$	0.26%
LBPH8N	$6.70/1.39\times10^{-4}$	0.19%

(b) EAST Kilo-second-Scale Discharge Testing
9 mV drift @ 1066s (< 0.1 % FSR);
ΔB/B >10× improvement over legacy units.

(c) 24-hour multiple continuous short-term discharges pulse drift testing
cumulative drift < 200 mV and stable real-time compensation.



Future work

Input impedance enhancement — Improving front-end impedance matching for long-distance transmission through optimized OP-stage design.

Thermal stability — Establishing quantitative models of temperature–drift coupling to increase environmental robustness.

Switching errors — Minimizing overlap-segment uncertainty caused by relay contact bounce by evaluating low-noise analog switch alternatives.

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