OVERALL PERFORMANCE OF THE HOUR-LEVEL ALTERNATING HYBRID INTEGRATOR

One of the key instruments for long-term magnetic diagnostic systems

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In January of this year, EAST achieved a high-performance plasma discharge lasting 1,066 seconds, approaching its maximum design target. As a key component of electromagnetic diagnostic system, the integrator faces a fundamental challenge: its input errors accumulate over time. EAST requires the integrator's total error to remain below 0.1% of the full-scale range (FSR). Among publicly reported results, F4E's fully digital integrator, originally designed for ITER's requirements, has demonstrated the best benchtop performance to date [1]. Tests indicate it meets ITER's stringent 500 μV -s/hour precision requirement in theoretical estimations. However, this solution exists several limitations including high sensitivity to thermal noise, complex architecture, and high costs, making it less suitable for large-scale deployment.

This paper presents a novel hybrid alternating integration architecture that employs two analog integrators to alternately perform real-time integration of input signals. The digital component learns and compensates for integration errors in real-time to enhance accuracy, effectively addressing inherent issues such as circuit saturation, and nonlinear errors. The self-learning capability eliminates the tedious tuning of conventional analog integrators while maintaining a simple, robust architecture. Test results show that this integrator delivers superior performance with significantly reduced error dispersion, while its hardware cost is less than one-third of the F4E prototype, making it well-suited for long-time high-precision integration.

Fig. 1(a) shows the optimized integration system, and its topology is illustrated in Fig. 1(b). A dual-parallel integrator operates alternately to avert saturation. During any cycle, only one INT_UNIT integrates the Rogowski-coil signal while another is reset subsequently connected to ground via a dummy load to characterize its drift characteristics. A τ -calibration algorithm equalises the time constants to within 0.05%. The microcontroller unit (MCU) subsequently concatenates the outputs from both INT_UNITs, producing a continuous, drift-compensated signal for the data acquisition system (DAS) and the plasma control system (PCS). A digital isolator decouples the DAC from the preceding circuitry, preserving signal integrity.

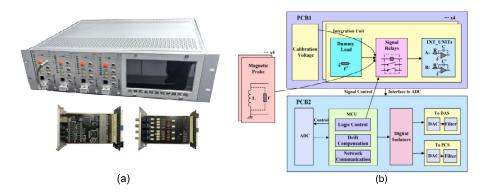


Fig. 1. Optimized integration system. (a) Boards and instruments (b) Topology of the dual-INT_UNIT alternating integrator.

Four integrator units underwent 104 bench-test runs, each lasting more than 4000s (Fig. 2(a)). The drift distribution of 4000s for all channels is shown in Fig. 2(b). Almost 99.1 % of the cycles maintained cumulative drift <0.1 % FSR (20 mV). At 2500s the optimized integrators achieved 100 % compliance with ITER's 500 μ V·s/hour target, outperforming the ITER directed F4E integrator prototype (97.2 %). Error dispersion ($\sigma \approx 5.6$ mV, $\mu \approx 0$ V) confirms excellent channel-to-channel repeatability. Fig. 2(c) presents a comparison of the 1000 s drift nonlinearity between the optimized integrator and existing integrators. The existing units exhibited

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significant nonlinear error (> 0.08 % FSR), whereas the optimized integrator reduced this error to below detectable levels (< 10 ppm). These data attest to the superior stability and suitability for ITER's integrator specifications.

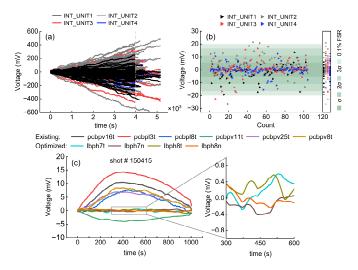


Fig. 2. Error dispersion characterization with nonlinearity validation and drift. (a) Integration drift characterization over 4000-second. (b) Error dispersion characterization of 416 tests. (c) Nonlinear drift of conventional and proposed system.

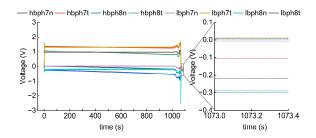


Fig. 3.Integration results of shot #150425 at each position.

During the EAST tokamak's 2024 winter plasma discharge campaign, four channels—LBPH7T, LBPH7N, LBPH8T, and LBPH8N—were dedicated to discharge tests, which were installed at positions symmetric to the corresponding HBPH prefixed channels—HBPH7T, HBPH7N, HBPH8T, and HBPH8N. As shown in Fig. 3, in a representative 1,066 s discharge (shot #150425), real-time compensated drift remained below 9 mV on every channel, whereas the existing integrators drifted more than 100 mV. The worst-case diagnostic accuracy (Δ B/B) of the optimized integrator complies fully with the 1 % specification, whereas existing integrators far exceed the allowable control-accuracy limits. Taken together with the other test results, these data confirm that the alternating, continuous-integrator satisfies the performance requirements for 1,000 s discharges on the EAST tokamak.

While meeting all accuracy specifications, each channel costs only 3,000–4,000 RMB, roughly 1/3 of the F4E prototype's price. Moreover, the input impedance has been increased to above $200 \,\mathrm{k}\Omega$, fully meeting the requirements of both BEST and ITER. These advances not only satisfy EAST's 1000 s discharge requirement but also furnish a production ready, high performance, and cost-effective option for ITER and the forthcoming BEST.

ACKNOWLEDGEMENTS

This work was supported by National Magnetic Confinement Fusion Program of China (No. 2015GB103000).

REFERENCES

[1] BATISTA, A. J. N., CAPELLÀ, L., NETO, A., HALL, S., NAYLOR, G., STEPHEN, A., SOUSA, J., CARVALHO, B., SARTORI, F., CAMPAGNOLO, R., BAS, I., GONÇALVES, B., ARSHAD, S., VAYAKIS, G., SIMROCK, S., ZABEO, L., F4E prototype of a chopper digital integrator for the ITER magnetics, Fusion Eng. Des. 123 (2017) 1025–1028.