

Prototype design of logic testing controller based on FPGA for interlock system

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The national project of experimental advanced superconducting tokamak (EAST) is an important part of the fusion development stratagem of China, which has fully superconducting tokamak with a non-circle cross-section of the vacuum vessel and the active cooling plasma-facing components. The safety and interlock system (SIS) is in charge of the supervision and control of all the EAST components involved in the protection of human and tokamak machine from potential accidents.

At present, the interlock systems of each plant system of the device are mostly implemented based on PLC, with a response time in the range of 10ms, and the interlock logic has been fixed. However, with the development of experimental requirements, new equipment and new plant systems with new interlock subsystems need to be added.

In the process of designing new interlock logic relationships and setting thresholds, parameters need to be frequently changed and logic relationships need to be frequently debugged, professional interlock control engineers are also required during the whole project.

The high-speed interlock logic testing controller designed in this article is a solution specifically designed for sub-millisecond high-speed acquisition and control, while requiring frequent changes in control logic project. It has 400MHz processor, 512MB storage and 256MB running memory, provides 16-channel AI, 4-channel AO, and 28-channel DIO. Suitable for medium-scale logic control (basic control logic quantity 50) applications. Users do not need programming skills, and they only need to use text language to edit logic in software such as spreadsheets. Statement such as: if $AI0 > 2.3$ or $AI3 \leq 0.4$ then set $AO1 = 2.34$ set $DO0 = 1$, the controller will perform the corresponding logical functions.

Users can change the operation logic of signal I/O through text editing without programming, and realize customized logic operation and control output, which can greatly reduce the workload of system debugging and use.

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