Prototype design of logic testing controller based on FPGA for interlock system

Presented by Zuchao Zhang[1.3]*

on behalf of EAST Central Control Team,

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ASIPP

- Introduction
- What's in it…
  - Logic Rationale
  - Hardware Structure
  - Software Design
  - Program Develop
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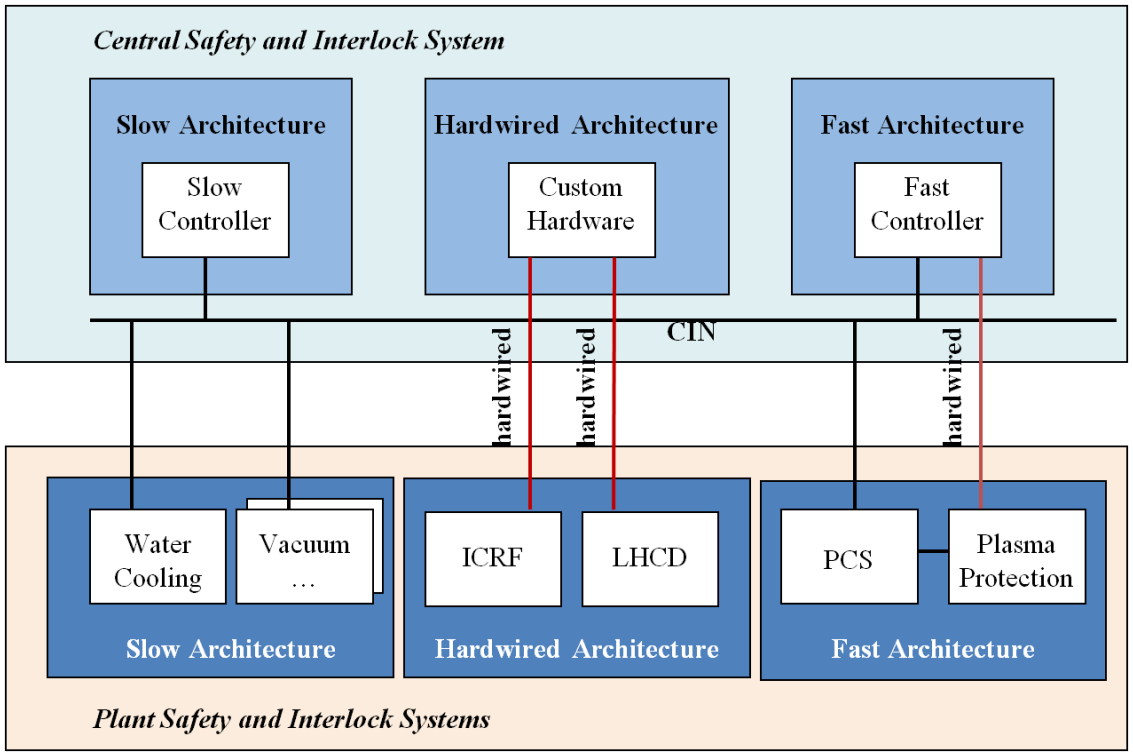
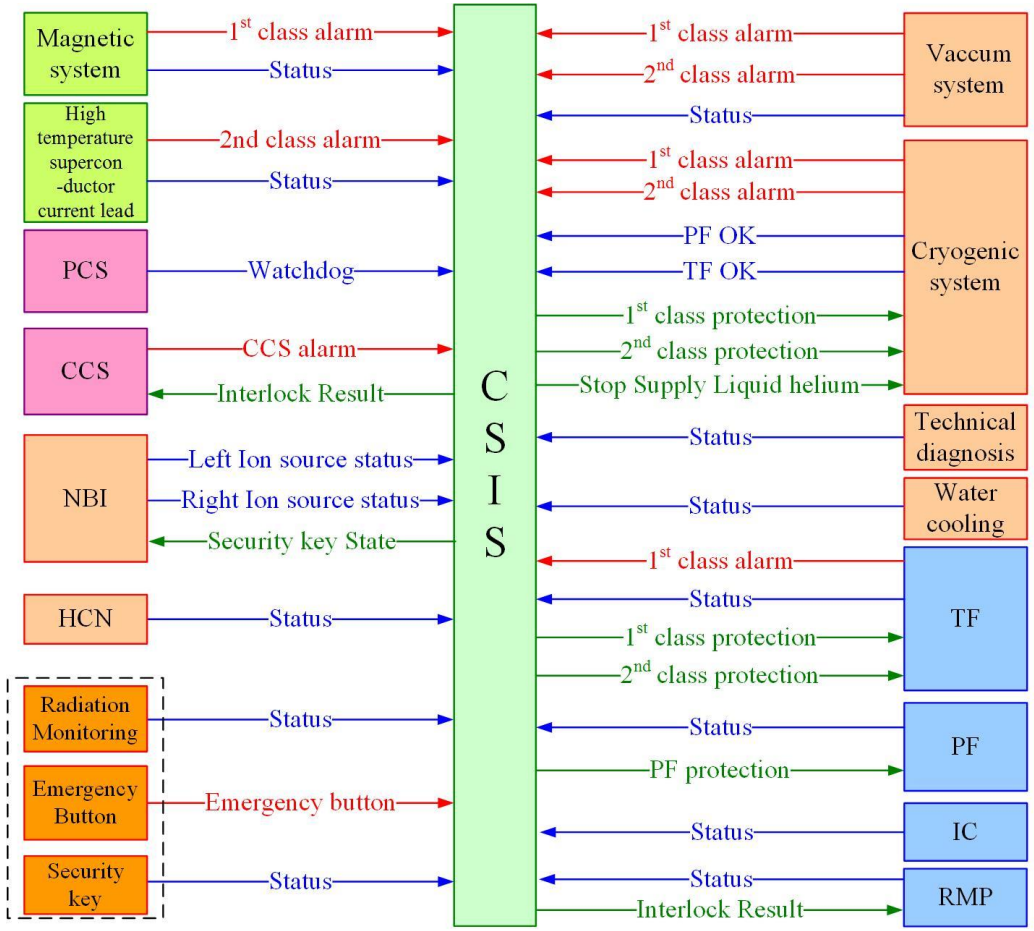
ASIPP

EAST Central Safety & Interlock System -- CSIS

- Scans subsystem status, provides protection signal, ensures personal and machine security during whole experiment.
- More stable supervisory and control operation.



EAST Safety and Interlock System horizontal layers



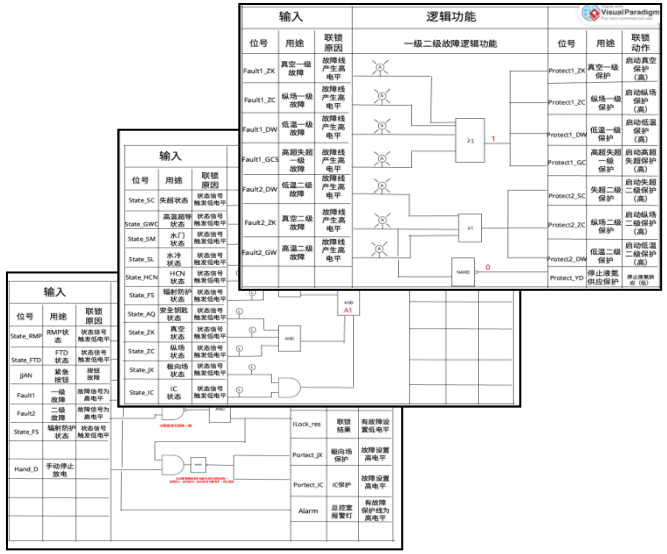
Interface between CSIS and plant systems

BACKGROUND

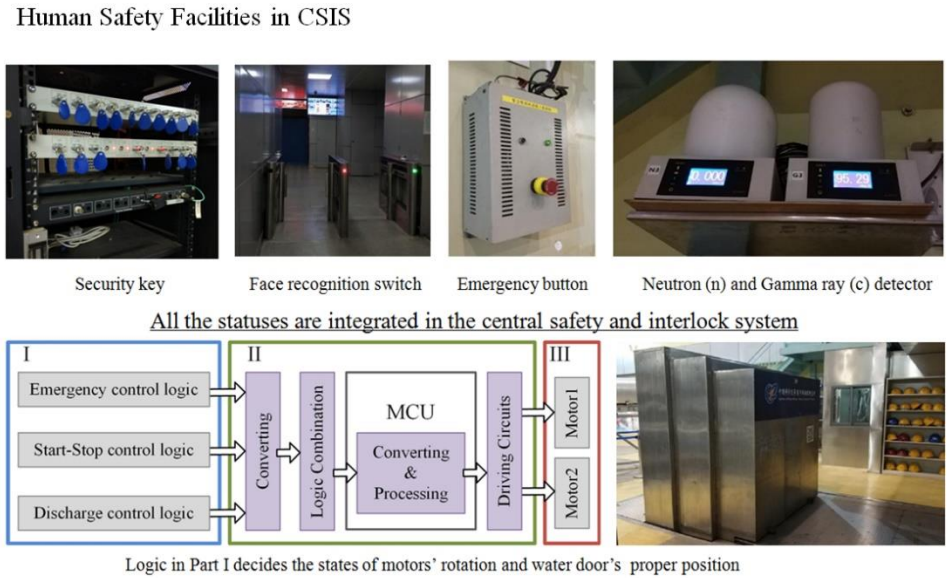
new EAST CSIS upgrades with:

- Reviews and upgrades some logical relationship and interface;
- Integrates several new features and plant systems, such as FTD (fishtail divertor), FRS(face recognition signal) , *etc.*;
- Uses SIL-3 safety integrity COTS hardware and configuration software;
- Redundancy mechanism make the system more stable and reliable.

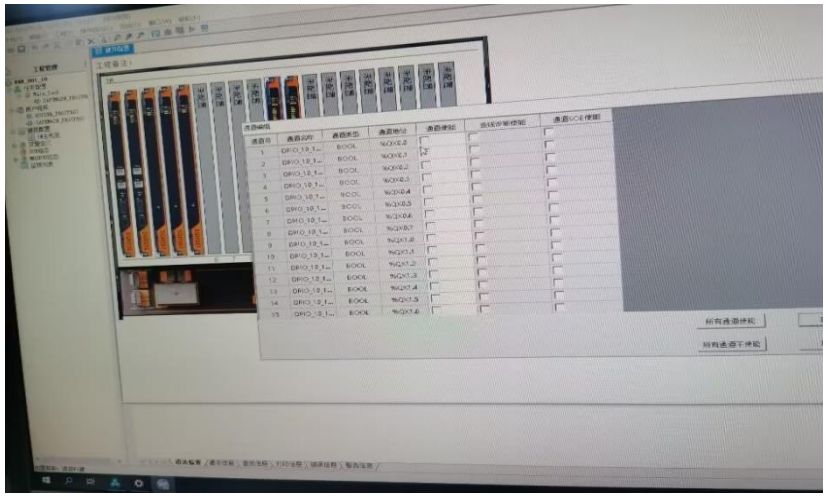
Hardware of new EAST CSIS



Main Logic Files for CSIS



Human Safety Facilities in CSIS



Configuration Software for CSIS

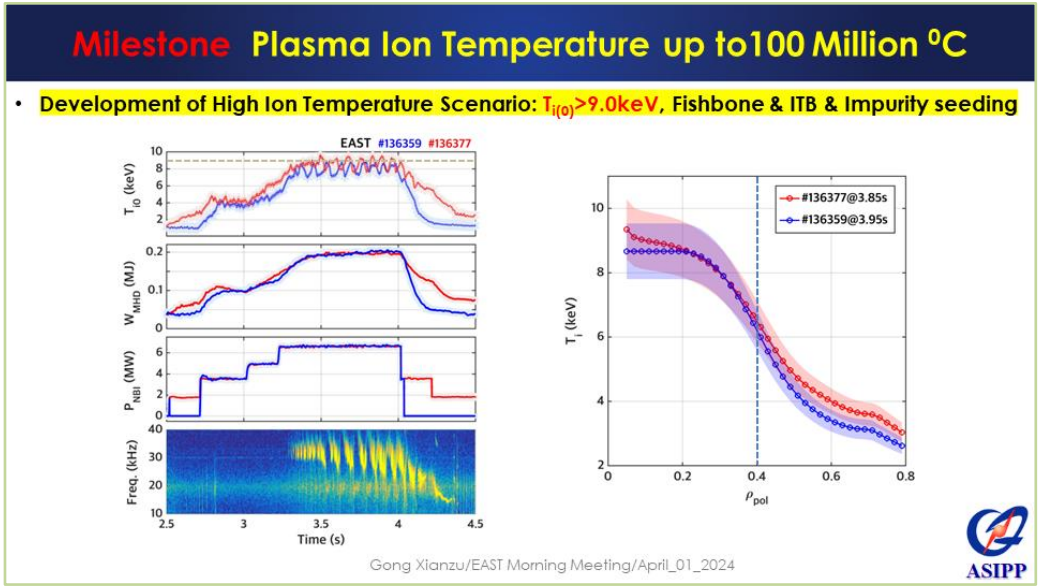
Motivation

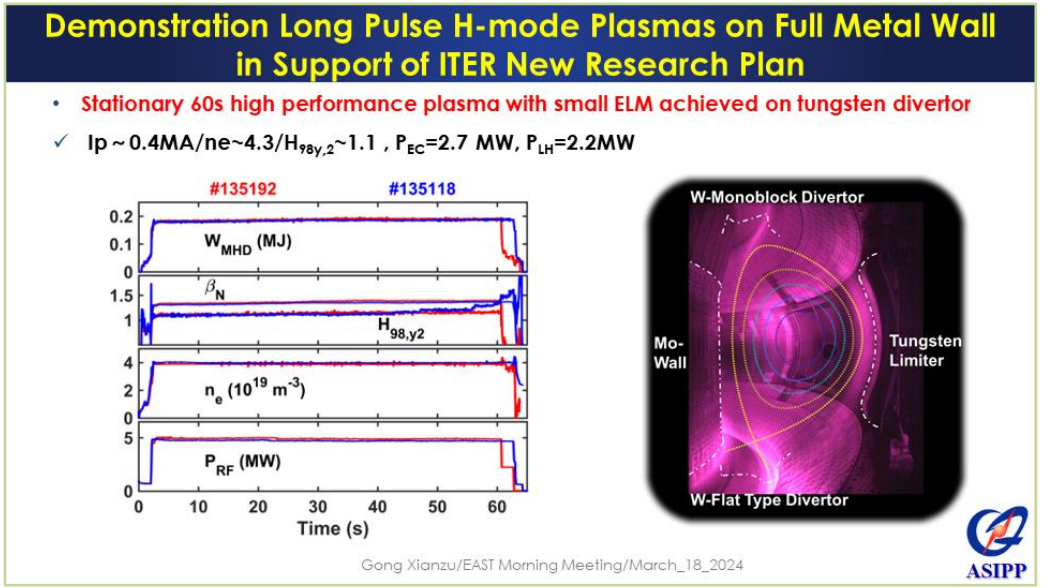
Ongoing EAST Experiments …

- **from December 2023 to now**
- **main goals**
  - **G1: Demonstration of long Pulse high performance plasmas with W-Divs in Support of New Baseline for ITER Research Plan**
  - **G2: High Power Operation by ICRH/NBI heating without Li-coating to enhance Ion temperature: PIN~6.0-10MW, Ti0>8.5keV**
- **more than 14,000 shots (from No.129314)**
- **7x24h, no long-term maintenance and repair**

No chance to validate and test the new CSIS

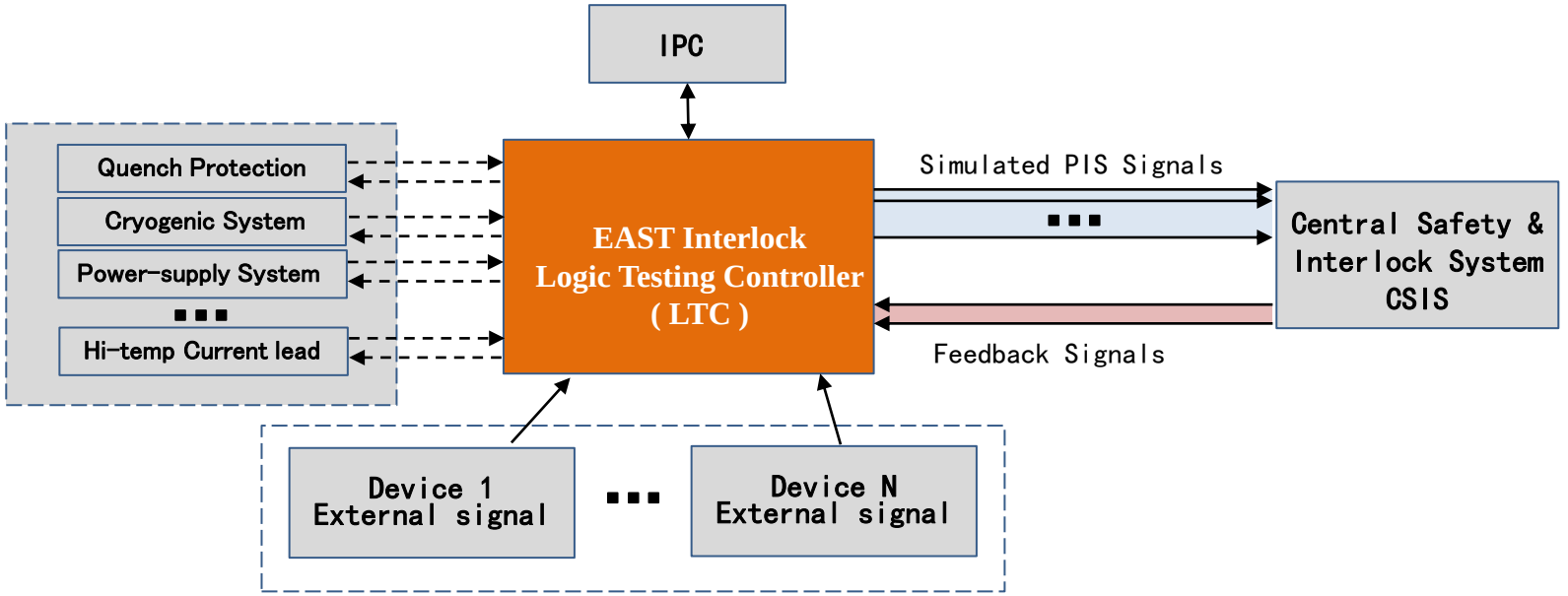
Logic Testing Controller (LTC)





Motivation

- A plant interlock system simulator, which one or several PIS could be simulated;
- A mini-CSIS, assists in verifying subsystem interlock functionality;
- A tool kit, tests the new changes to the software and functions before released when they are considered stable.



Interface functions among LTC and other systems

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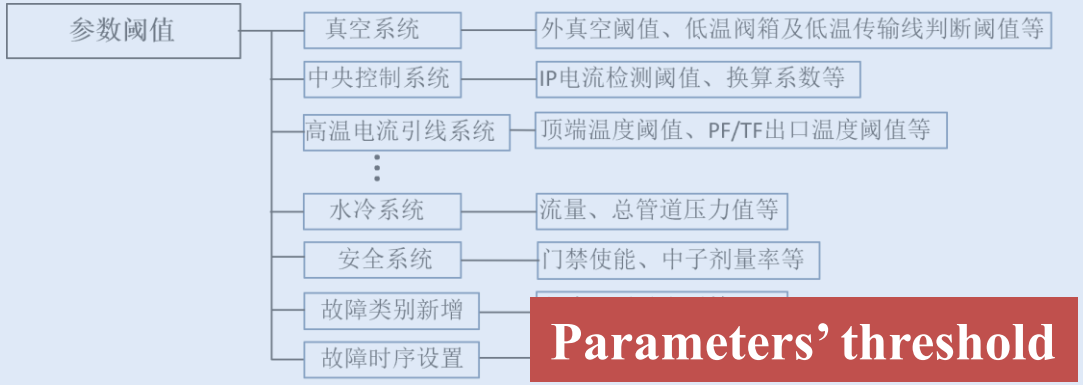
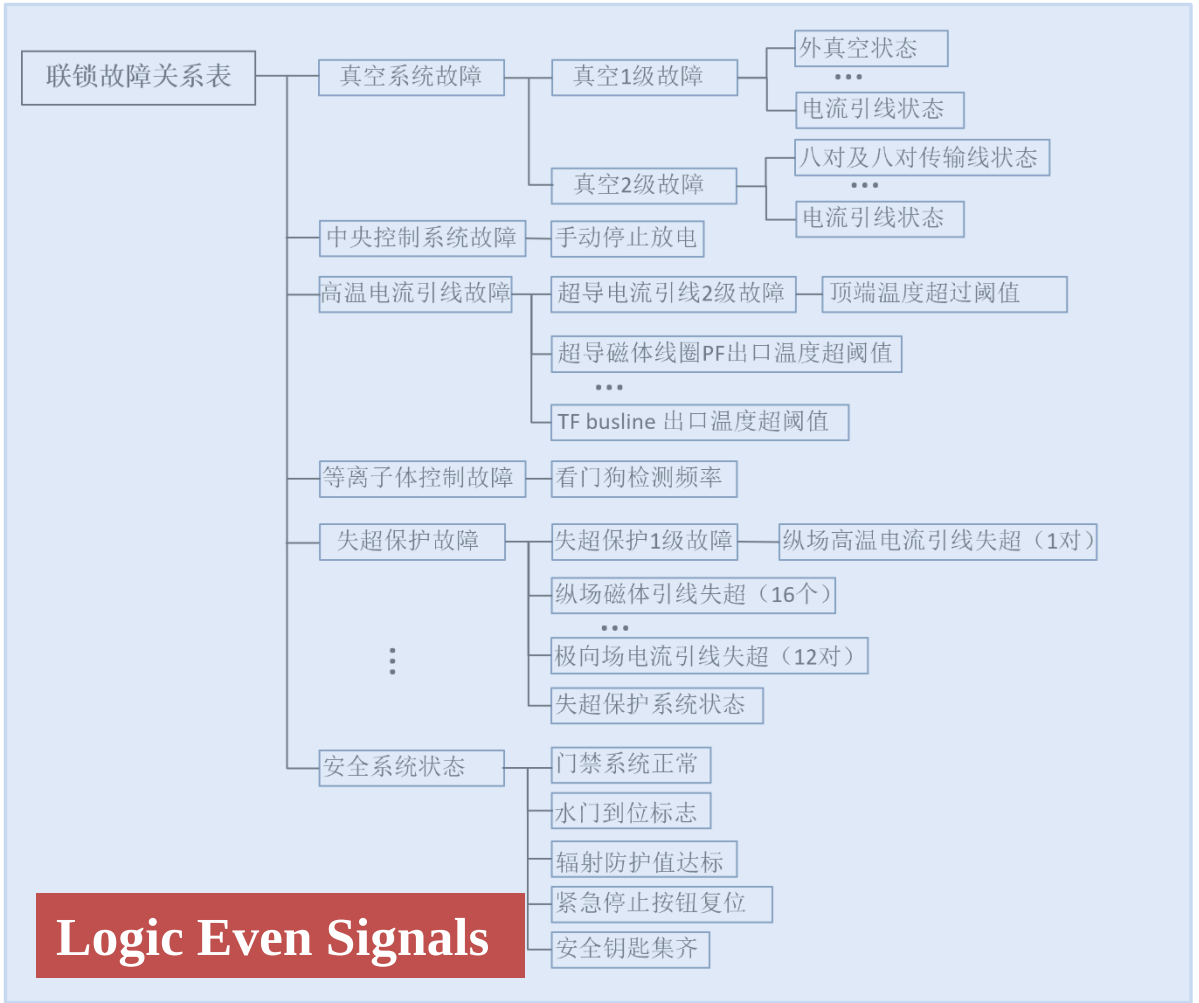
Logic Rationale

Interlock logic information :

- Collects **ALL** interlock details, over 20 EAST plant systems/devices ;
- **Correct** threshold value setting for key parameters, ~ 260 ;
- Signal types:
  Status/Alarm/Protection;
- Alarm classification, ~2.

Signal	Value	Response
Status	High	OK
	Low	alarm
1st class alarm	High	1st class protection
	Low	OK
2nd class alarm	High	2nd class protection
	Low	OK
Protection	High	actuator
	Low	null

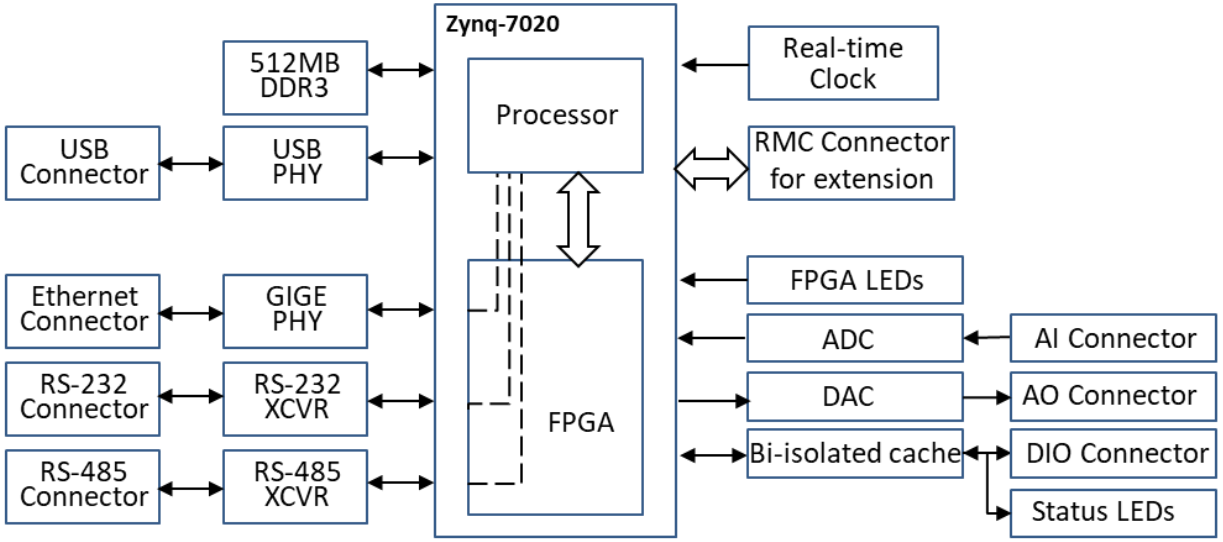




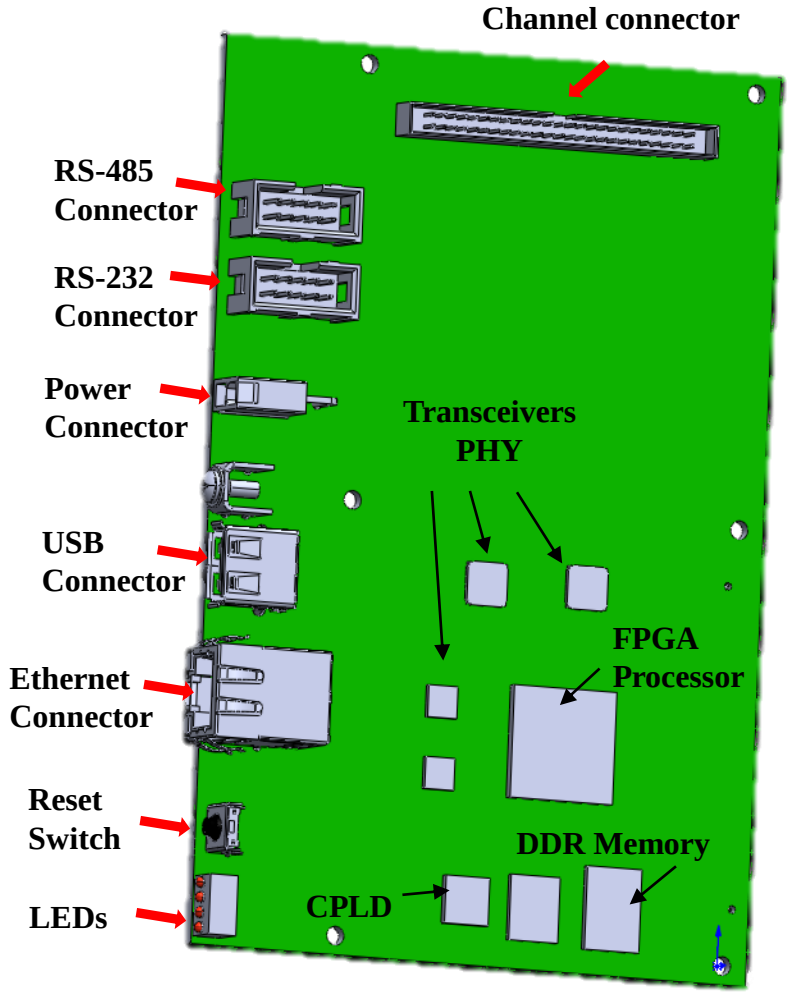
Hardware Structure

Hardware features:

- Processor: Xilinx Zynq-7000, XC7Z020 All programmable SoC, ARM Cortex-A9, 512MB, Linux Real-time (32 bit) OS;
- Reconfigurable FPGA: 85,000 logic cells, 106,400 flip-flops, 560 KB available block RAM;
- Connectors: Ethernet Port, RS-232 Serial Port, RS-485 Serial Port, 16 single-ended AI channels, 4 AO channels, 96 DIO

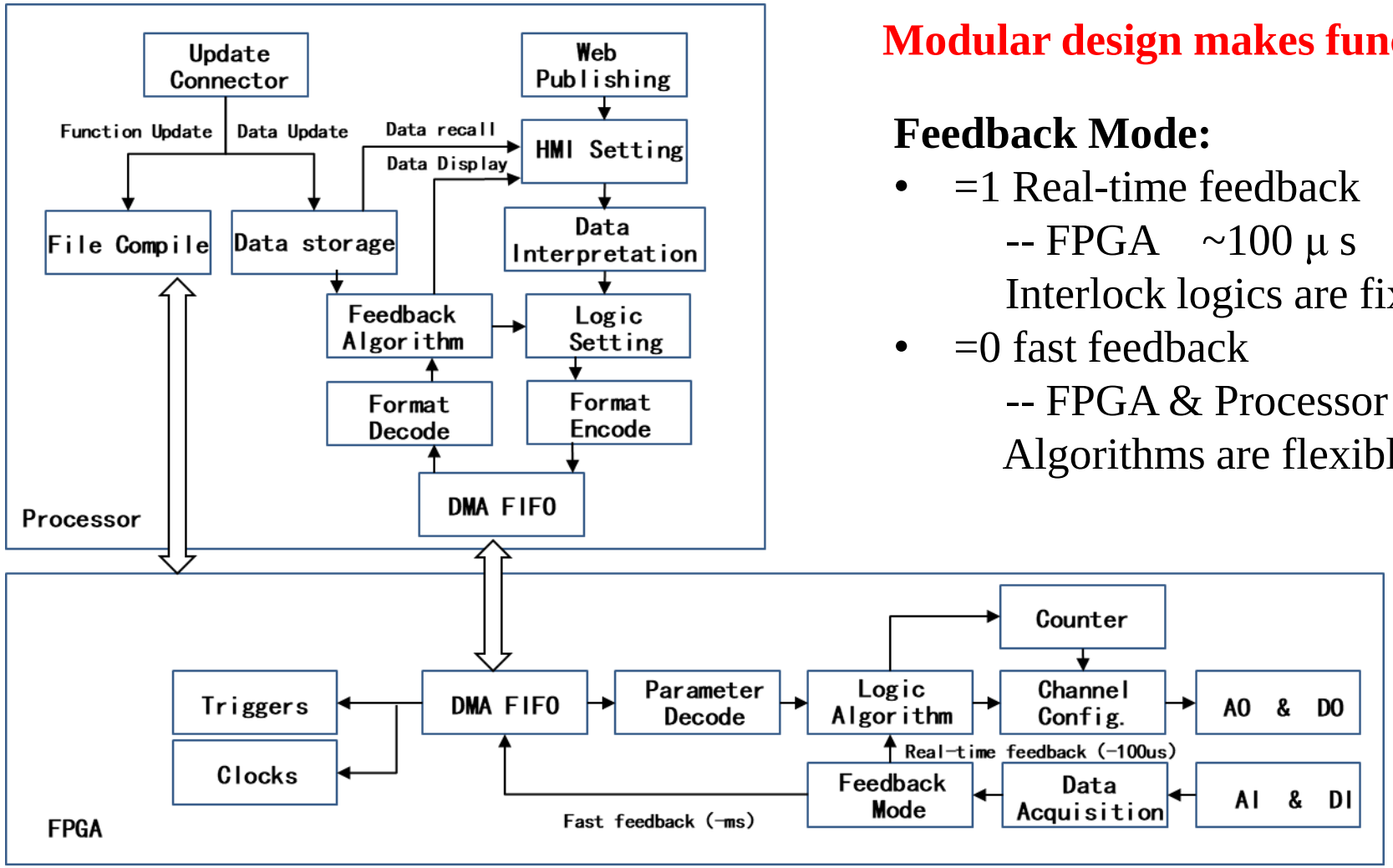


Structure of LTC hardware



LTC Hardware Model

Software Design



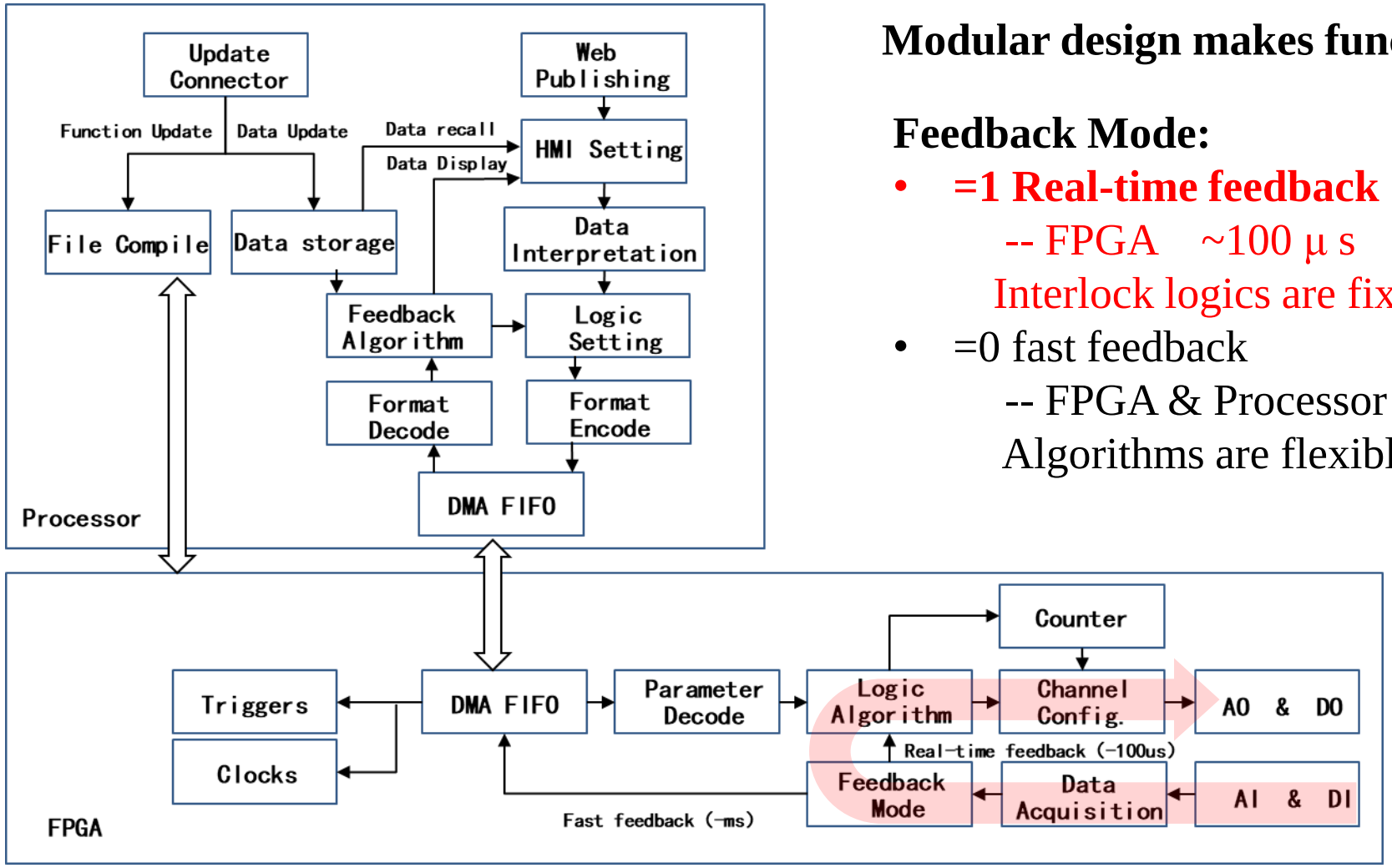
Modular functions for an LTC

Modular design makes functional upgrades much easier

Feedback Mode:

- =1 Real-time feedback
  -- FPGA ~100 μ s
  Interlock logics are fixed » Mini-CSIS / fast CSIS
- =0 fast feedback
  -- FPGA & Processor ~ ms
  Algorithms are flexible » PIS simulator

Software Design



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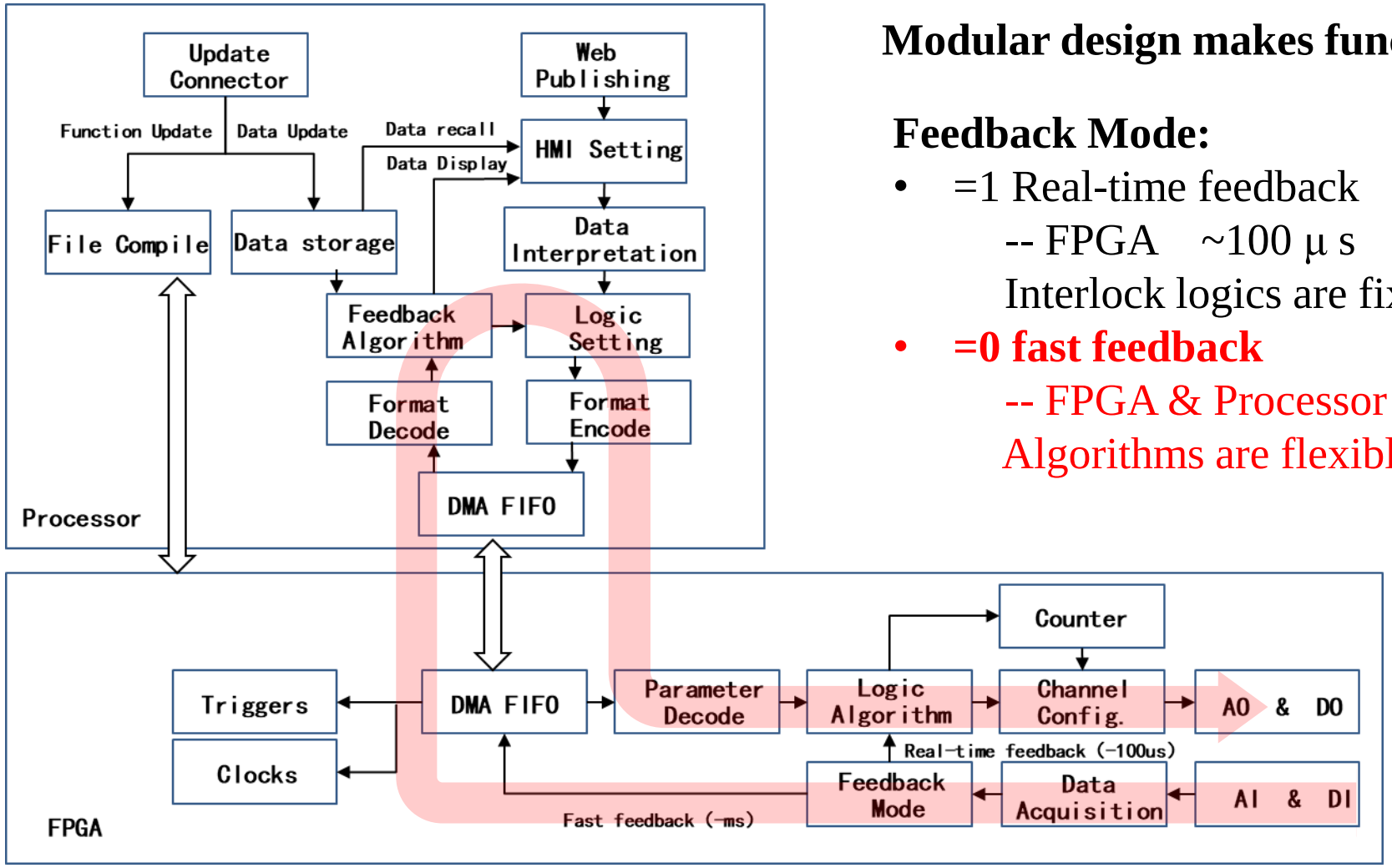

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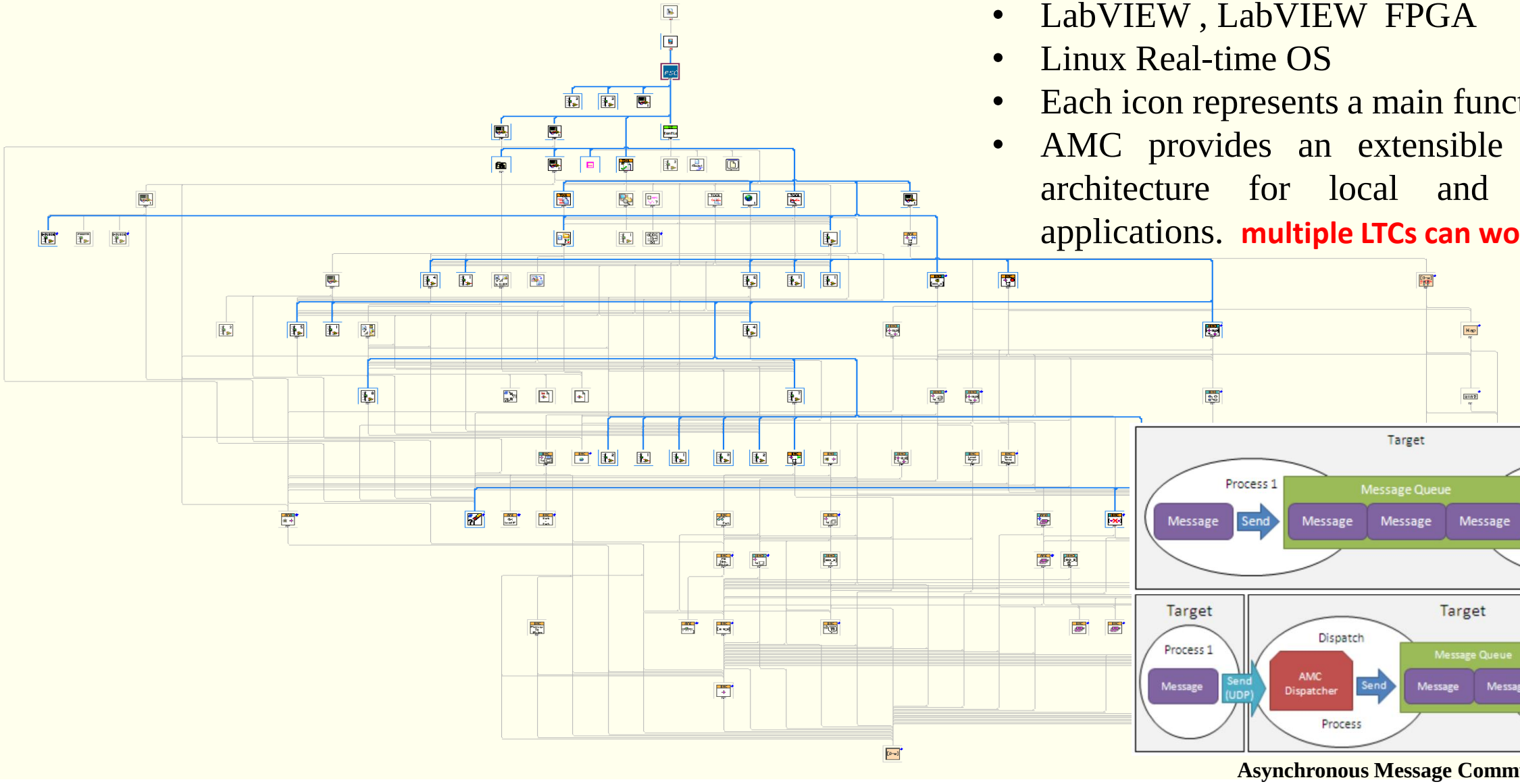
Program Develop

Program information

- LabVIEW , LabVIEW FPGA
- Linux Real-time OS
- Each icon represents a main function
- AMC provides an extensible messaging architecture for local and distributed applications. **multiple LTCs can work together**

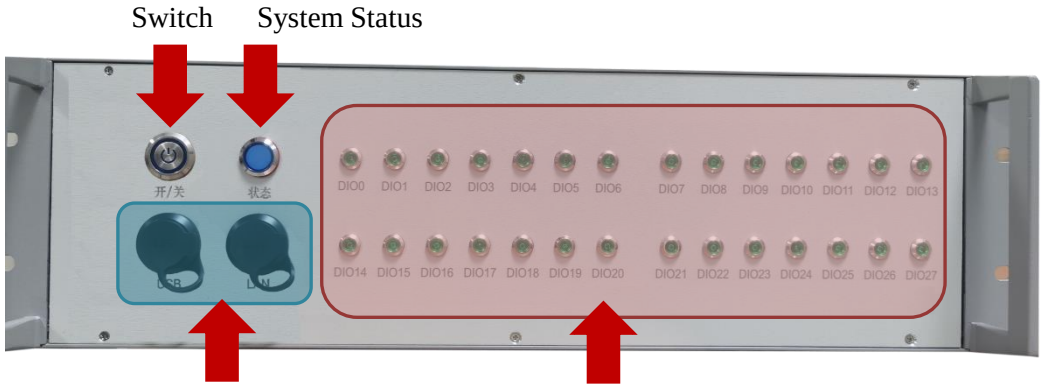


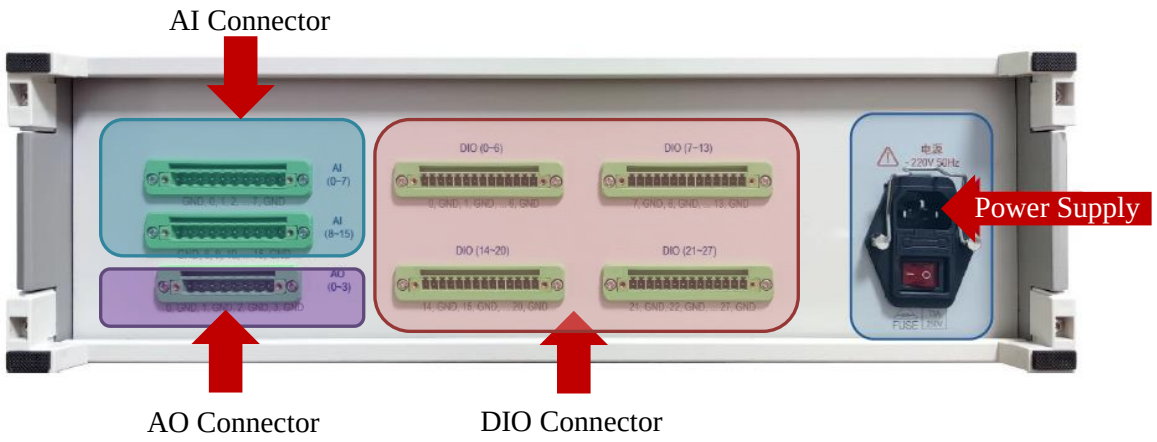
Main.vi hierarchy in an LTC

Asynchronous Message Communication

Device Assemble

Font Panel of LTC





Rear Panel of LTC

Top View of LTC

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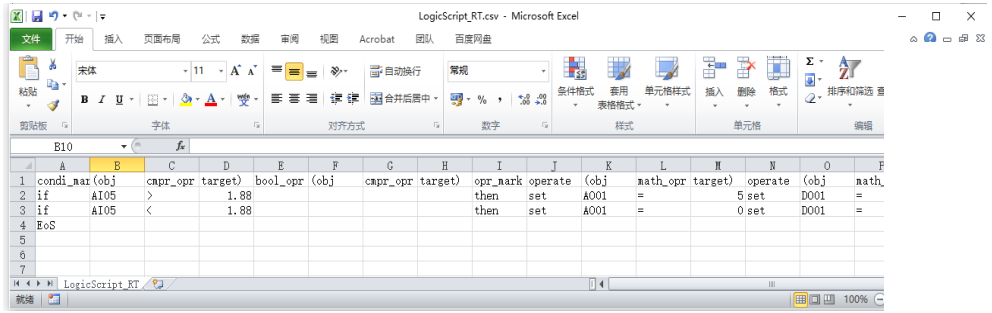
Basic functional testing

- Frequent parameter setting modification, frequent debugging of appropriate thresholds, repeatedly logic test

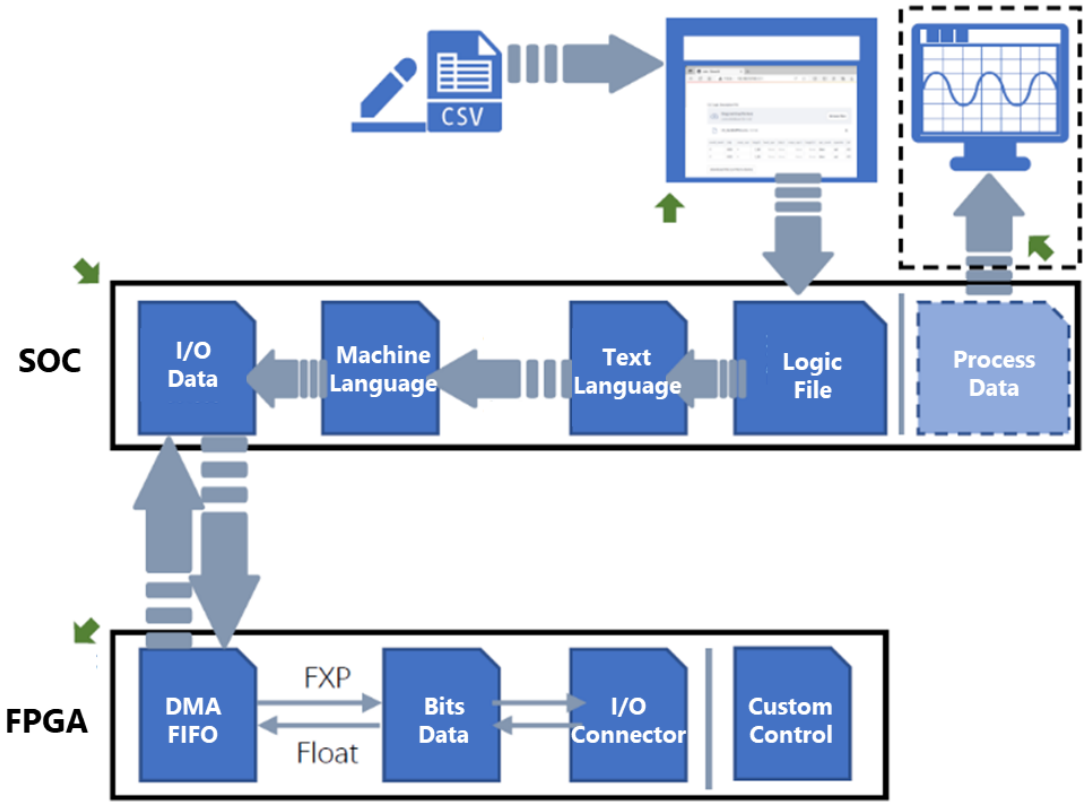


Logic configuration spreadsheet

- Users do not need programming skills,
  use text language to edit logic in spreadsheet.
  Statement such as:

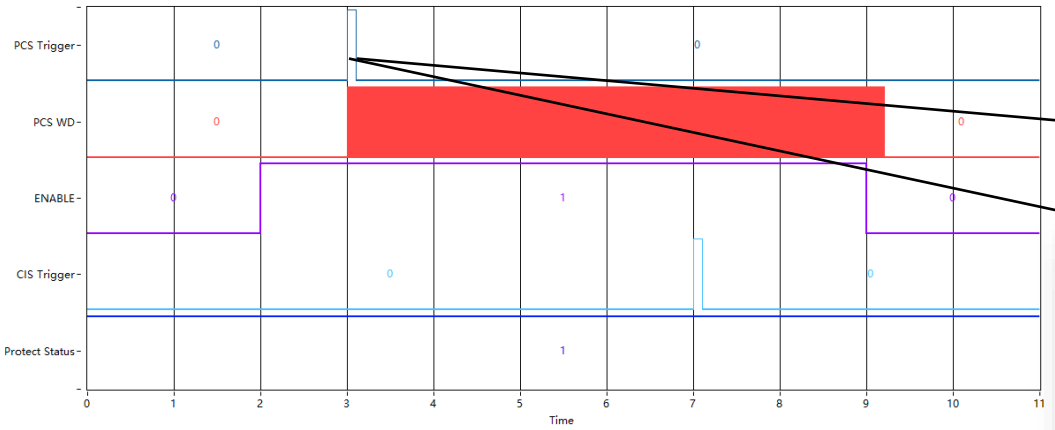
  if AI5 > 1.88 then set AO1 = 5 set DO0 = 1
  if AI5 < 1.88 then set AO1 = 0 set DO0 = 0

- Users can change the operation logic of signal I/O through text editing without programming, and realize customized logic operation and control output, which can greatly reduce the workload of system debugging and use.

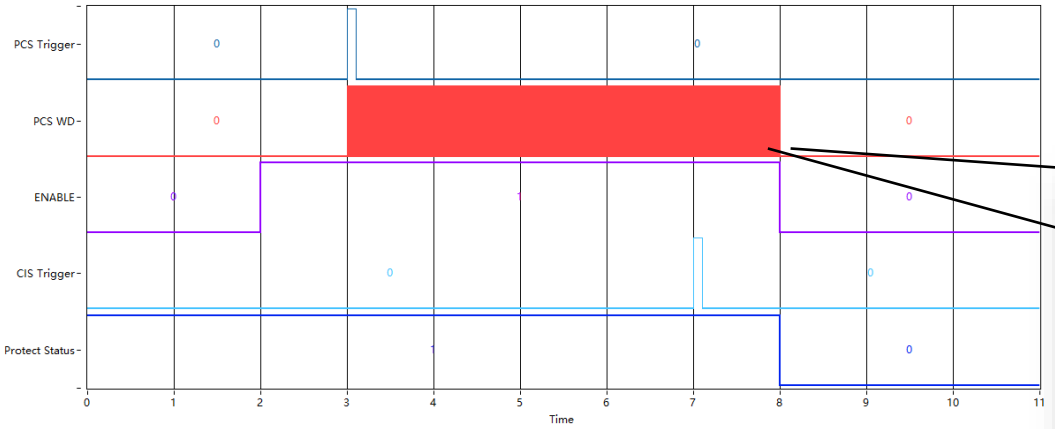


Data transmission process

PCS simulator function test - simulation



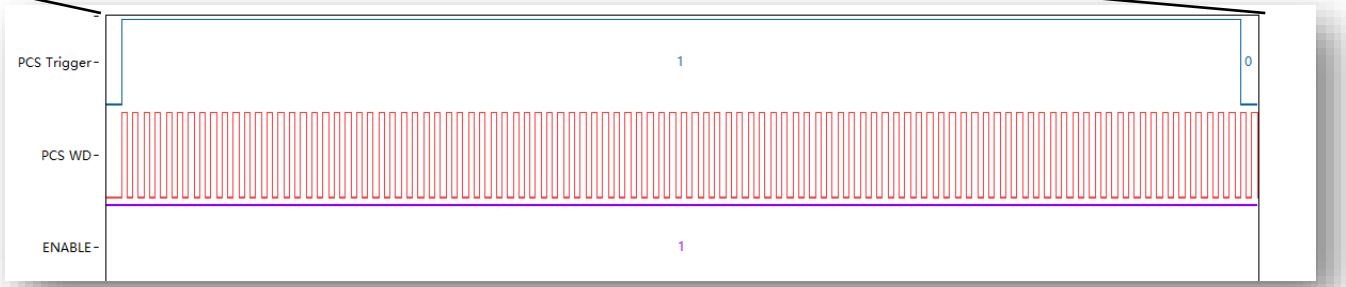
Signal relationship under normal conditions



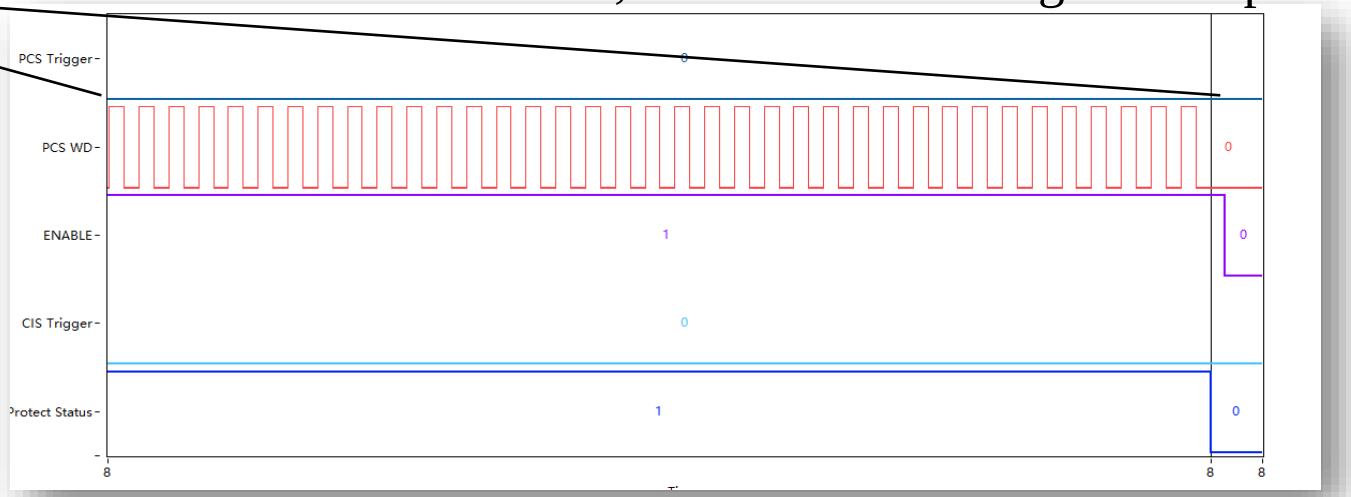
Signal relationship under unnormal conditions

Signal list

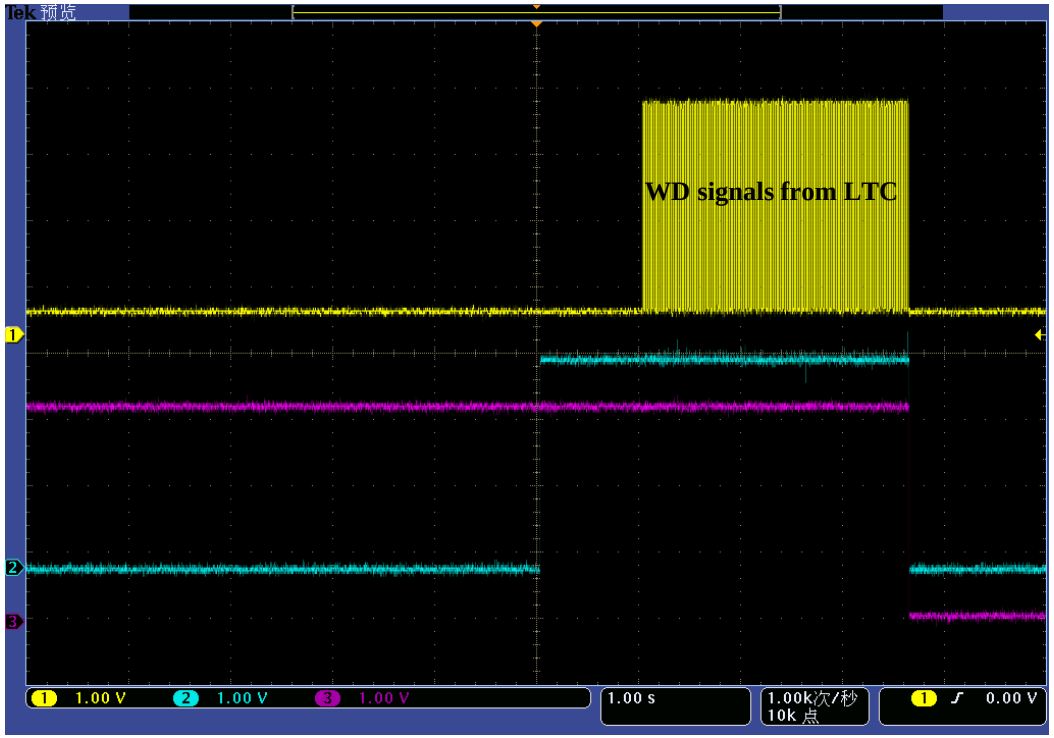
- PCS trigger, length width 10ms;
- WD 1 cycle = 200 μ s;



- Enable, follow with discharge status;
- CIS trigger, length width 10ms;
- Protect status, can lead to discharge interruption.



PCS simulator function test - in reality



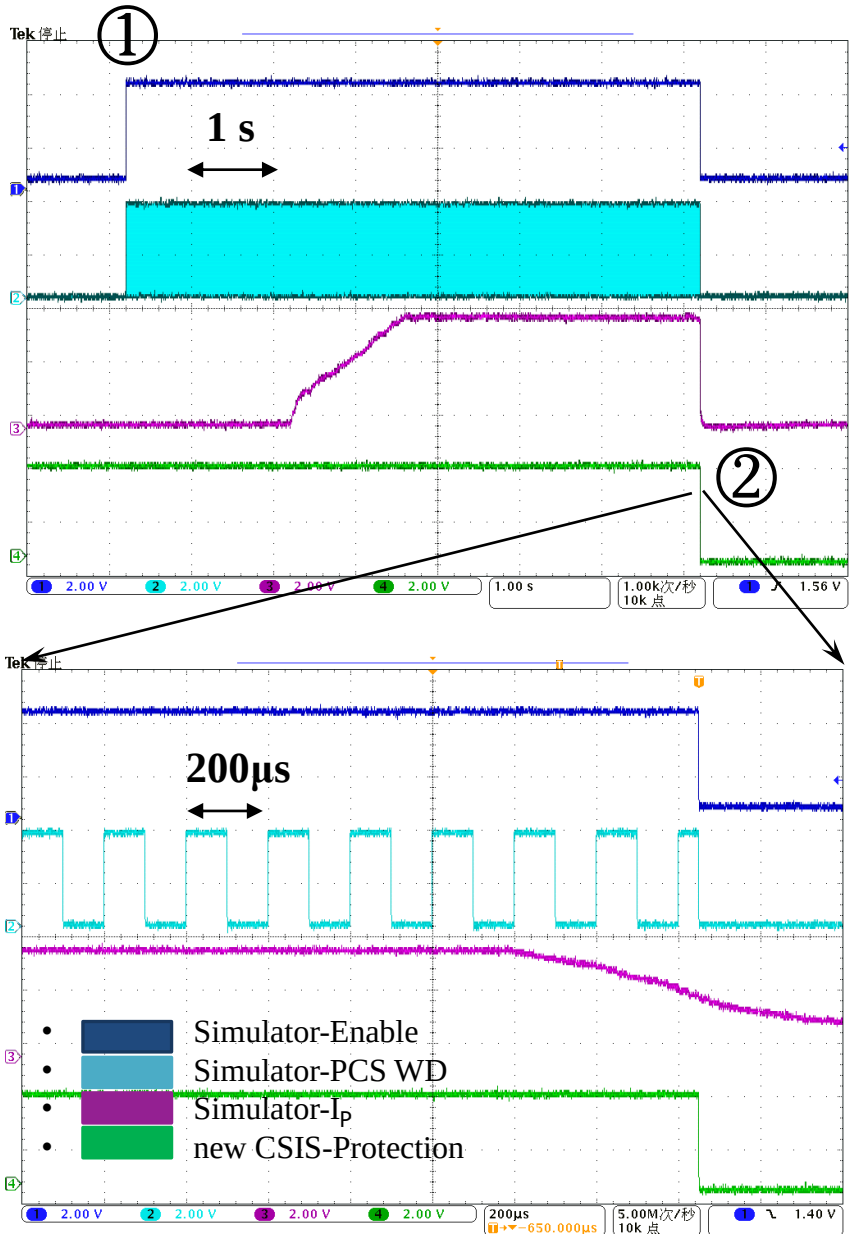
Data archived by oscilloscope

Contents: WD signal terminated prematurely

Pre-set parameters:
- Discharge length: 6 s
- PCS trigger time: -1s
- PCS work length: 2.6s

- Simulator-PCS WD, WD signal terminated prematurely.
- Simulator- Enable, follow the discharge status.
- new CSIS Protection, shows abnormal interlock status, lead to discharge interruption.

New CSIS test-plasma current detection



Data archived by oscilloscope

① 1 LTC generates an enable signal, it represents the length of discharge under normal conditions.

2 Enable signal activate Simulator-PCS, and output watchdog signal, cycle 200 µ s.

3 LTC generates a plasma current signal at preset time (-2s), it simulates the process of plasma discharge.

4 At the beginning, all the states are normal, and new CSIS-Protection output signal to PIS is high.

② 3 Simulator-Plasma current signal value decrease.

4 New CSIS detects a sharp signal changes, triggers the interlock algorithm, fans out protection signals to PIS

1 Protection signal turn to 0 means the discharge is terminated, so Simulator-Enable signal end. Waiting …

2 On receiving protection signal, PCS stops working, and the WD output is 0.

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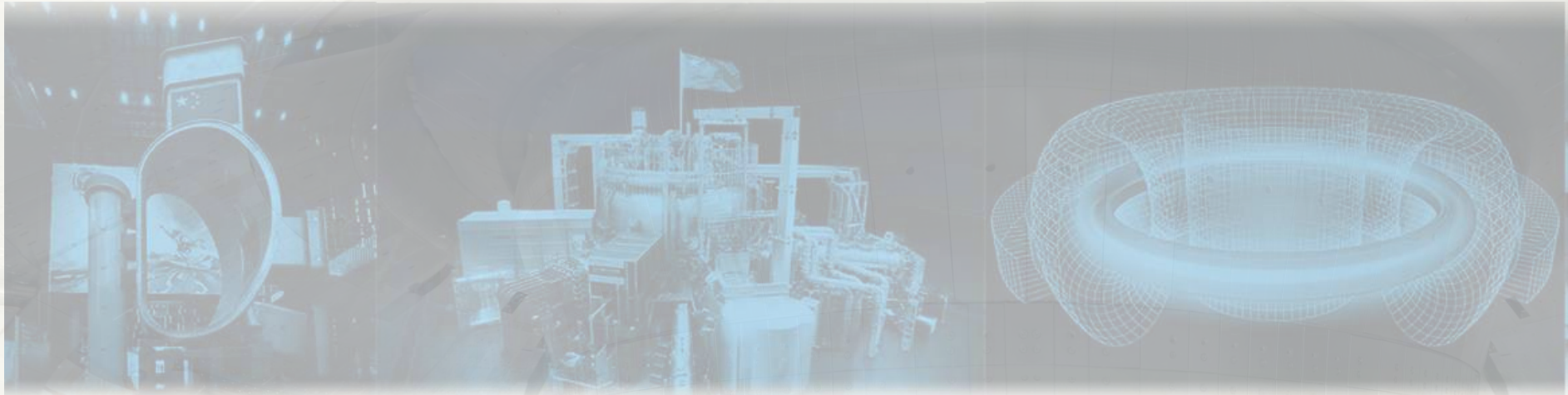
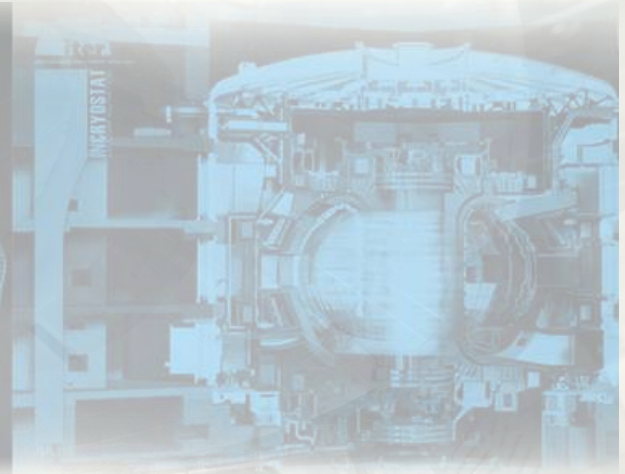
Summary

Logic Testing Controller

- LTC has comprehensive EAST PIS interlock logical details, all of subsystems have been involved;
- LTC is a good tool kit to test the new CSIS before released as PIS simulators;

Outlook

- More features will be added, such as touch screen HMI, fiber optic interface, *etc.*;
- Optimizing work will be conducted for BEST central interlock system.

Thank you !