

Summary on Machine Control Sessions

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Outline

- Short taxonomy
- Interlock systems
- Precision timing
- I&C architectures
- Final remarks

No. 7 Presentations out of 50 → 14%

- Fusion experiments
 - no. 4 - ITER and ITER-related (#13 #24 #31 #37)
 - no. 1 – JT-60SA (#34) (busy in tokamak commissioning)
 - no. 1 – KSTAR (#28)
 - no. 1 – LHD (#21)
- Application domains
 - no. 3 – Interlock systems (#13 #28 #31)
 - no. 1 – Precise timing (#21)
 - no. 2 – I&C architectures (#24 #34)
 - no. 1 – Networking for remote experimentation (#37)
 - *will be summarized in Remote Participation Sessions*

Challenges for application of IEC61508 to systems for investment protection containing FPGA Off-the-Shelf components: the ITER Interlock System Fast Architecture use case

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As built design of the control systems of the ITER full-size beam source SPIDER in the Neutral Beam Tests Facility

Gabriele Manduchi 24

Event reconstruction using KSTAR FIS event counter in hot KSTAR plasma Myungkyu Kim 28

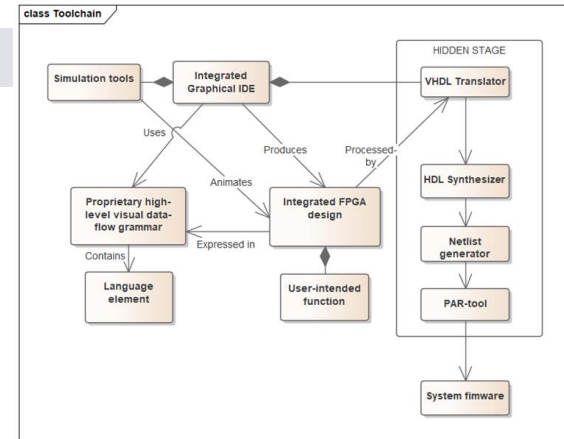
The final design of the ITER Interlock Discharge Loop Interface Boxes (DLIB) and its compliance with the IEC 61508 standard. Ignacio Prieto Diaz 31

Data management system for the plant monitoring data in JT-60SA Riho Yamazaki 34

Design study of REC-XPOZ network for ITER Remote Experimentation Centre (REC) Shinsuke Tokunaga 37

Interlock systems

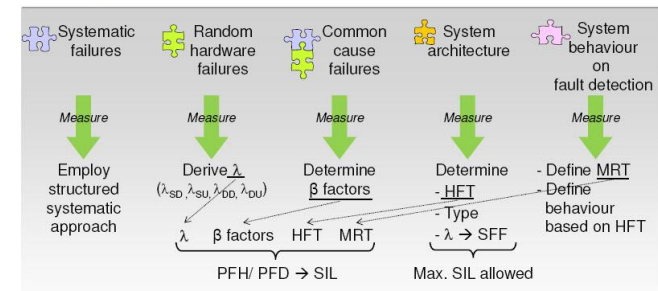
- Emphasis on IEC 61508 technical standard
 - Not surprising as it is the top standard for Functional Safety of Electrical/Electronic/Programmable Electronic Safety-related Systems
 - Life-cycle
 - Safety Integrity Level - reliability
- Speed vs reliability
 - Huge efforts to achieve both
 - High speed (μs range)
 - high reliability (SIL3 - Low demand mode: average probability of failure on demand $\text{PFD} \geq 10^{-4}$ to $< 10^{-3}$)
- FPGA firmware reliability
 - IEC 62566:2012 Nuclear power plants – I&C important to safety - Development of HDL-programmed integrated circuits for systems performing category A functions
- A common interface called DLIB (Discharge Loop Interface Box), which is the base of the coordination between the hardwired loop and the different users, has been designed up to final validation to be used for the fast energy discharge protection for ITER magnets



Fast Interlock Architecture (#13)

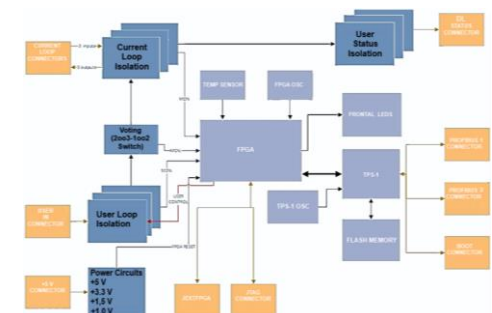
Way to Hardware SIL

TUV NORD



How to get λ ? → Quantitative analysis, e.g. FMEA, FTA, Markov, etc.

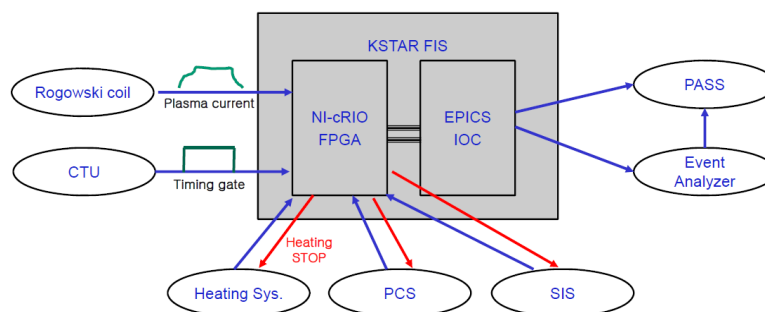
Reliability analysis (#31)



DLIB architecture (#31)

arch – Culham UK (virtually), 5-8 July 2021

- Need to record events with appropriate time-base to discriminate (KSTAR FIS)
 - An event counter has been developed by using FPGA to collect events with a resolution of $10\ \mu\text{s}$ during plasma discharge of KSTAR



FIS block diagram (#28)

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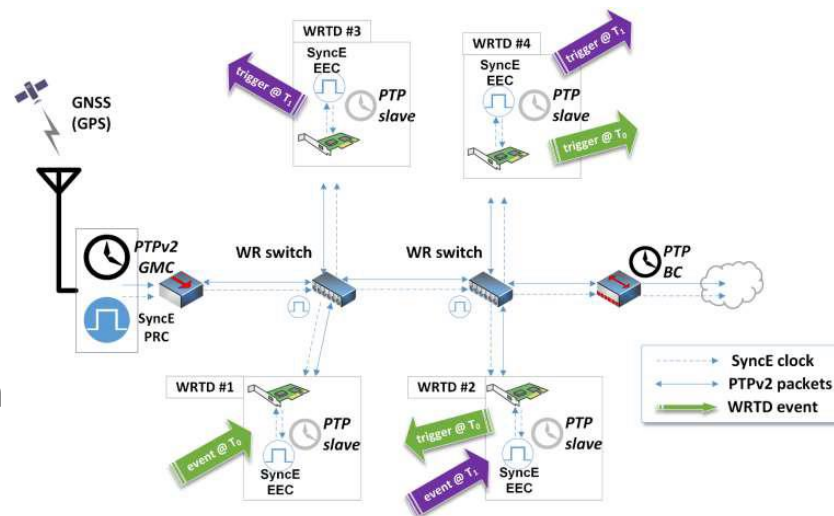
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- Need of Gsample/s data acquisition systems
 - fast & highly synchronized diagnostics, e.g. reflectometry
 - Demo?

- White Rabbit provides sub ns synchronization
 - Draft standard IEEE1588-2019 - High Accuracy Default Profile
 - Requires Synchronous Ethernet
 - Provides trigger events
 - Lacks trigger grouping and divided clocks (see #21)



White Rabbit Trigger Events (#21)

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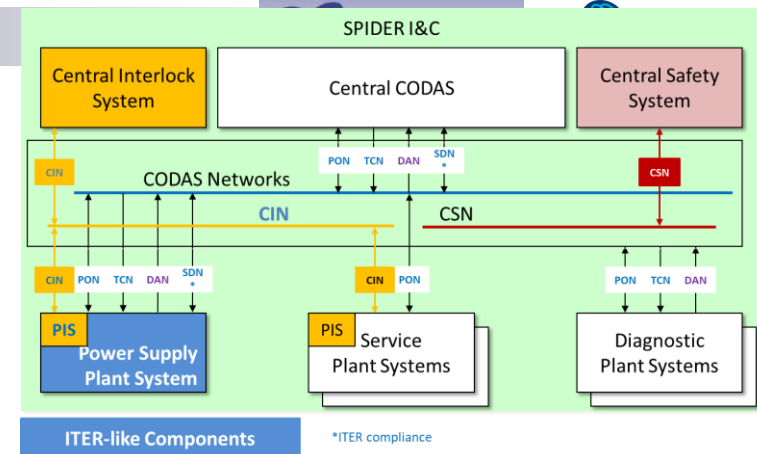
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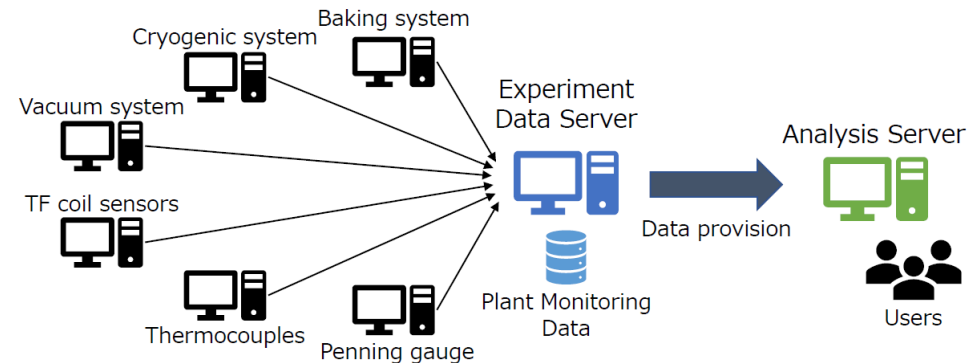
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- ITER-like I&C architecture
 - Neutral Beam Test Facility
 - ITER I&C compliancy of HNB is mandatory



- Plant data monitoring system
 - A data system has been developed to acquire all the monitoring data for all the plant systems continuously for 24 hours with frequencies about 1 HZ in a same time base for JT-60SA tokamak.

Three-tier ITER-like I&C architecture (#24)



Plant monitoring data flow (#34)

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- Increasing usage of FPGA
- Looking forward to new machines (and up-to-date architectures/technologies?)
 - JT-60SA (QST)
 - DTT (ENEA)
 - SPARC (MIT)

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Thank you very much
Looking forward to meeting you in person at
the 2023 14th IAEA TM