

Framework Design of the CFETR PCS Simulation Verification Platform

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To support the CFETR PCS development and discharge scenario optimization, the PCS Simulation Verification Platform (PCS-VP) is designed and developed. The framework of PCS-VP is divided into three layers, as device layer, function layer, and presentation layer, which follows the layered and modular design principles. The device layer interacts with the operating system and provides hardware driver modules to support the hardware-in-the-loop simulation between the platform and the PCS or other device subsystems. The function layer provides interpreters and solvers for system simulation, as well as powerful model libraries and interfaces with third-party models. The presentation layer provides a visual modeling and simulation environment. The model library of PCS-VP provides great convenience for plasma system simulation modeling. It includes a mathematical library for mathematical modeling and basic calculations, a plasma simulation library customized with a variety of plasma controllers, actuators, and plasma response models, and some auxiliary modules such as signal publishing and subscription module, event injection and exception capture module. In addition, the PCS-VP supports customized modules. Users can write function modules in C language or construct models by Simulink. At present, the prototype of PCS-VP, including visual simulation environment and part of the model library, has been developed based on python. And the poloidal coil current control and power supply models of EAST were constructed using the platform, the closed-loop control test between these models had consistent results with that in MATLAB/Simulink, which verified the feasibility of the framework design.

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