

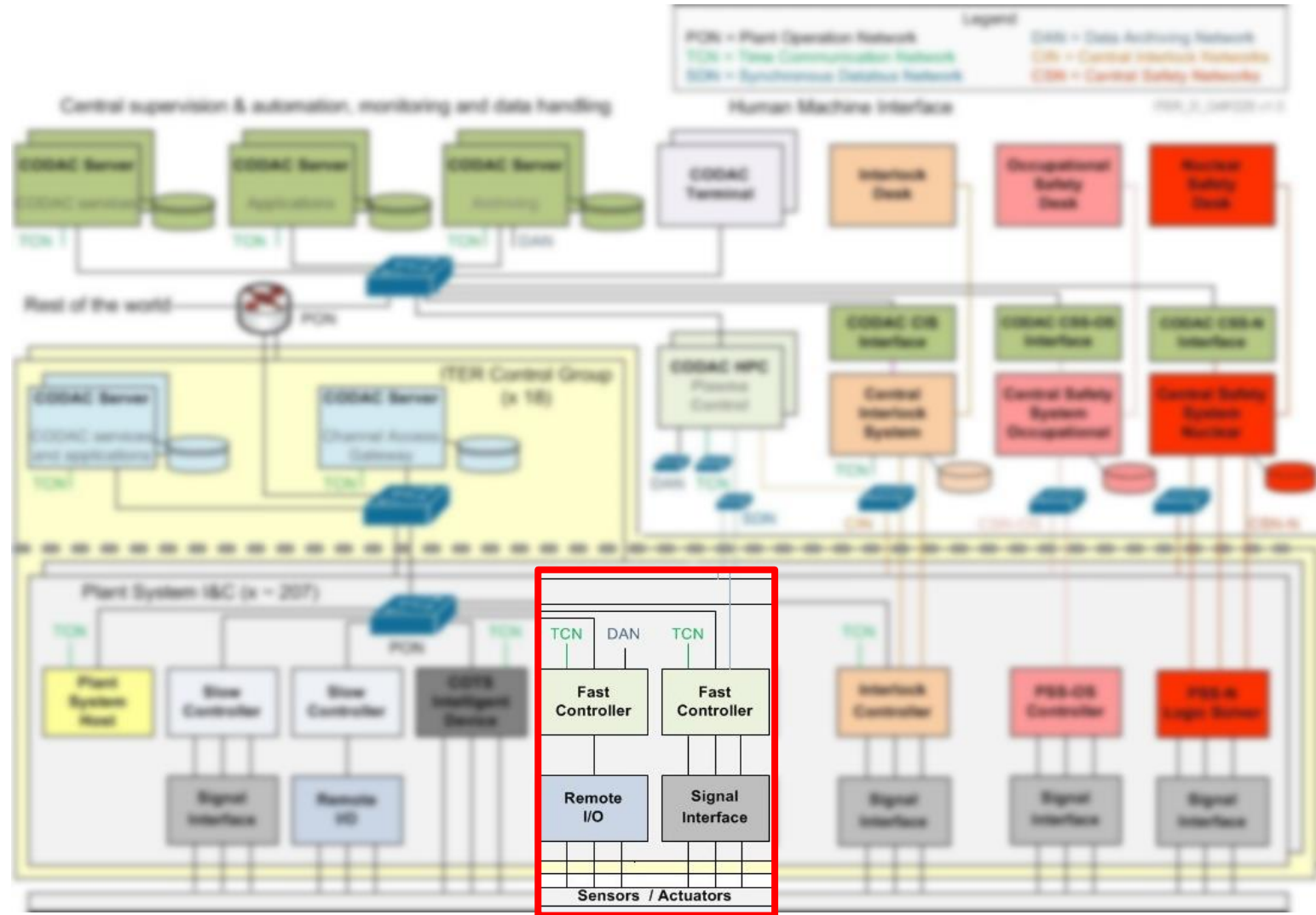
Implementation of an FPGA-based DAQ and Processing system for Neutron-Diagnostics using Nominal Device Support, OpenCL and MTCA

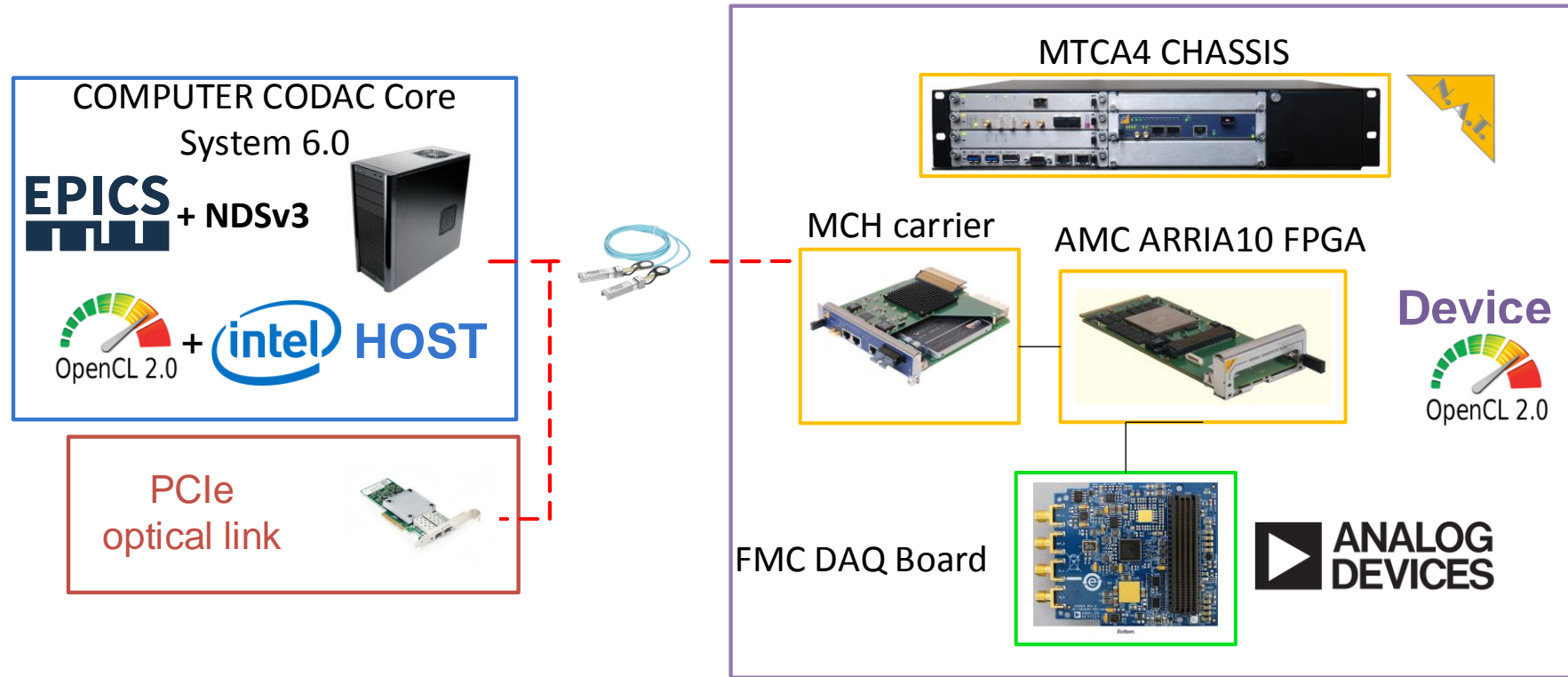
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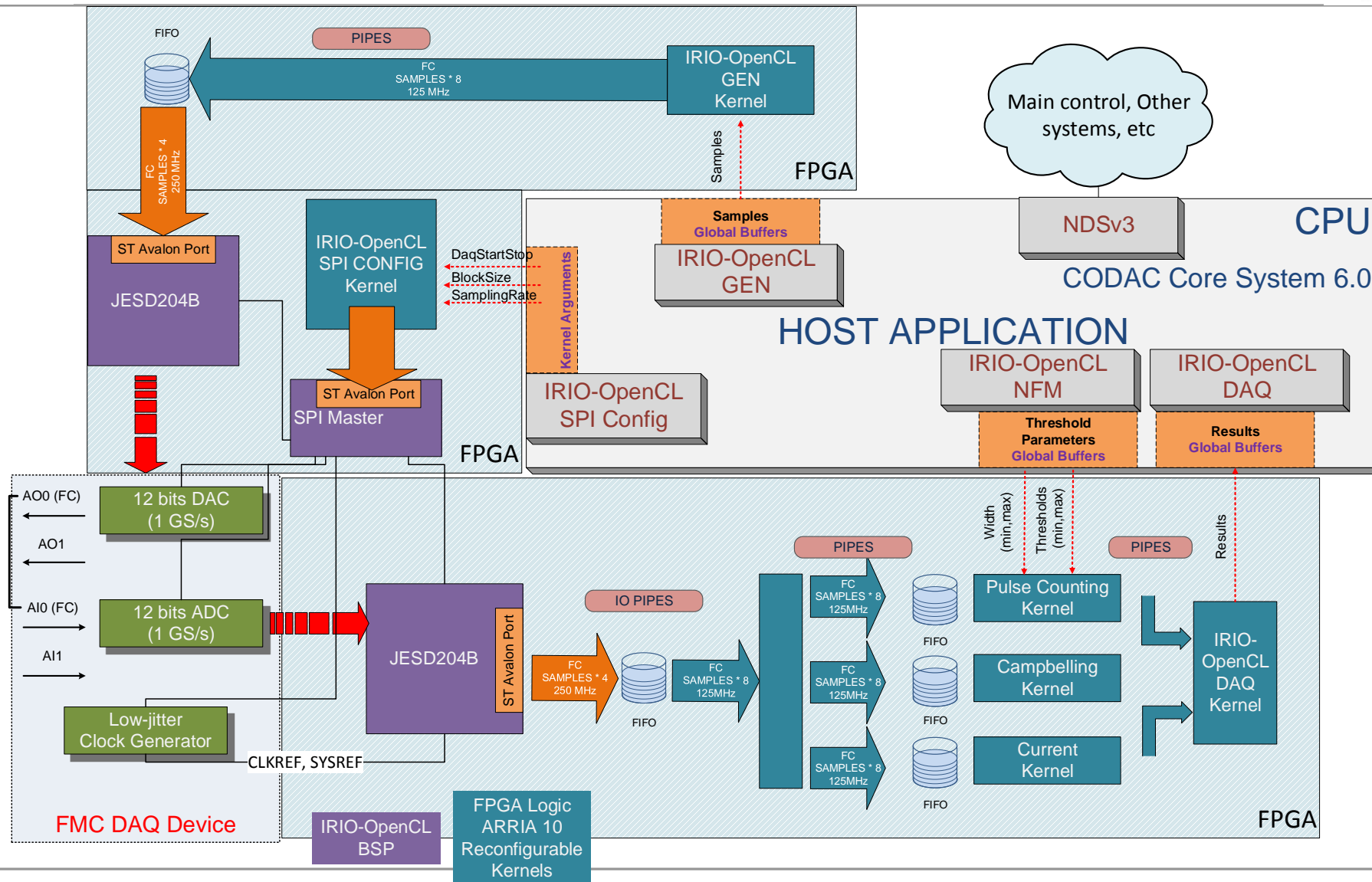
Context





- PC + PCIe + MTCA + AMC + (PROCESSING) + (I/O)
- **Thursay mini and poster on NDSv3!!**

Implementation Overview



- The Intel OpenCL compiler generates an efficient pipeline to process data at very high throughput. HW is described using OpenCL language.
- FPGA resource utilization with all the IRIO-OpenCL functionality is less than 50%.
- The hardware is managed using NDSv3 allowing an easy connection to EPICS.
- The complete platform is integrated in ITER CODAC Core System.
- **Today's topic: OpenCL is being extensively used for machine learning applications.**

More details in the plenary oral:

490. Methodology to standardize the development of FPGA-based intelligent DAQ and processing systems on heterogeneous platforms using OpenCL

Thursday 9:00

Implementation of an FPGA-based DAQ and Processing system for Neutron-Diagnostics using Nominal Device Support, OpenCL and MTCA

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Thanks for your attention!!

This work was supported in part by the Spanish Ministry of Economy and Competitiveness, Projects Nº ENE2015-64914-C3-3-R and Madrid regional government (YEI fund), Grant Nº PEJD-2018-PRE/TIC-8571.

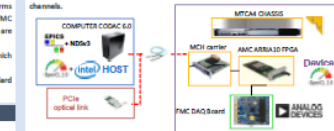
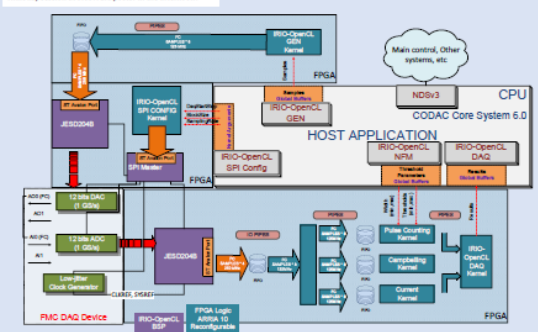


Implementation of an FPGA-based DAQ and Processing system for Neutron-Diagnostics using NDS, OpenCL and MTCA
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HIGHLIGHTS
• Neutron flux measurement is a good use case to test the implementation of hardware in FPGA using OpenCL-based tools. The algorithm is well-known, and benefits from high sampling rate devices.
• A database of pulses is created, generating the waveforms either by a signal generator or using the DAC in the FMC module. The acquired signal by ADC in FMC module are processed in an Intel® FPGA Arria10 FPGA.
• With the FPGA, the algorithm is divided into kernels, which are synthesized to be executed in parallel.
• The solution is implemented using MTCA 4 standard platform.

HARDWARE
MTCA chassis with a carrier hull, which provides an optical PCIe interface. The processing device is the NLAZ (AMC) module NANC-Arria10-FMC board. This board consists of an Intel® FPGA Arria10 and includes an FMC (FPGA Mezzanine Card) connector where the AD-DAQ27FMC-EBZ module providing two 105/5k ADC channels together with two 105/5k DAC channels.

METHOD
The methodology to be described in contribution ID 494. Thursday session at 9.00! And poster in the afternoon!

ACKNOWLEDGEMENTS
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CONCLUSION
 > The Intel OpenCL compiler generates an efficient pipeline to process data at very high throughput. HW is described using OpenCL languages.
 > FPGA resource utilization with all the RIO-OpenCL functionality is less than 50%.
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Poster location: P/2-4
15/05/2019