Implementation of an FPGA-based DAQ and Processing system for Neutron-Diagnostics using Nominal Device Support, OpenCL and MTCA

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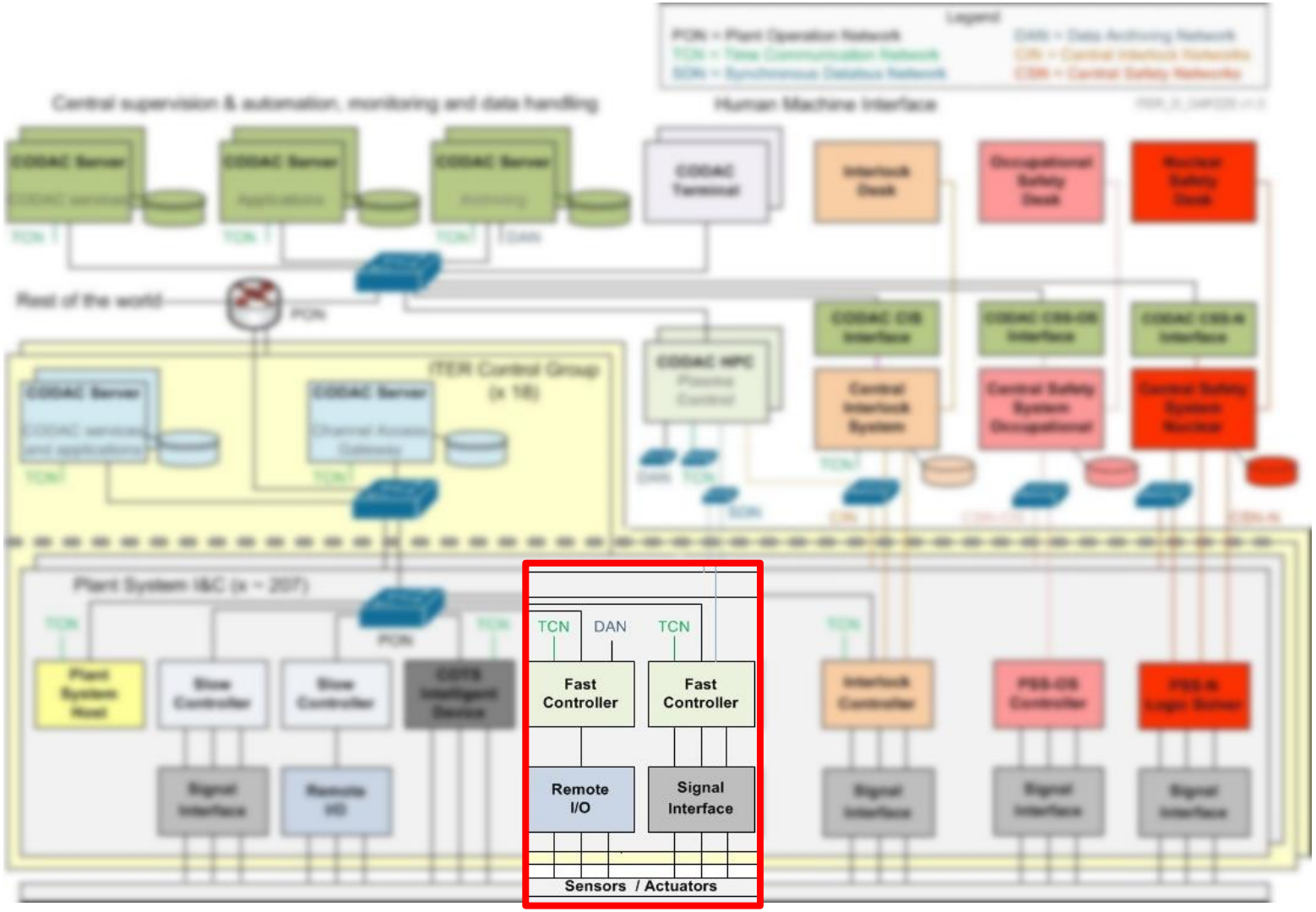
Context



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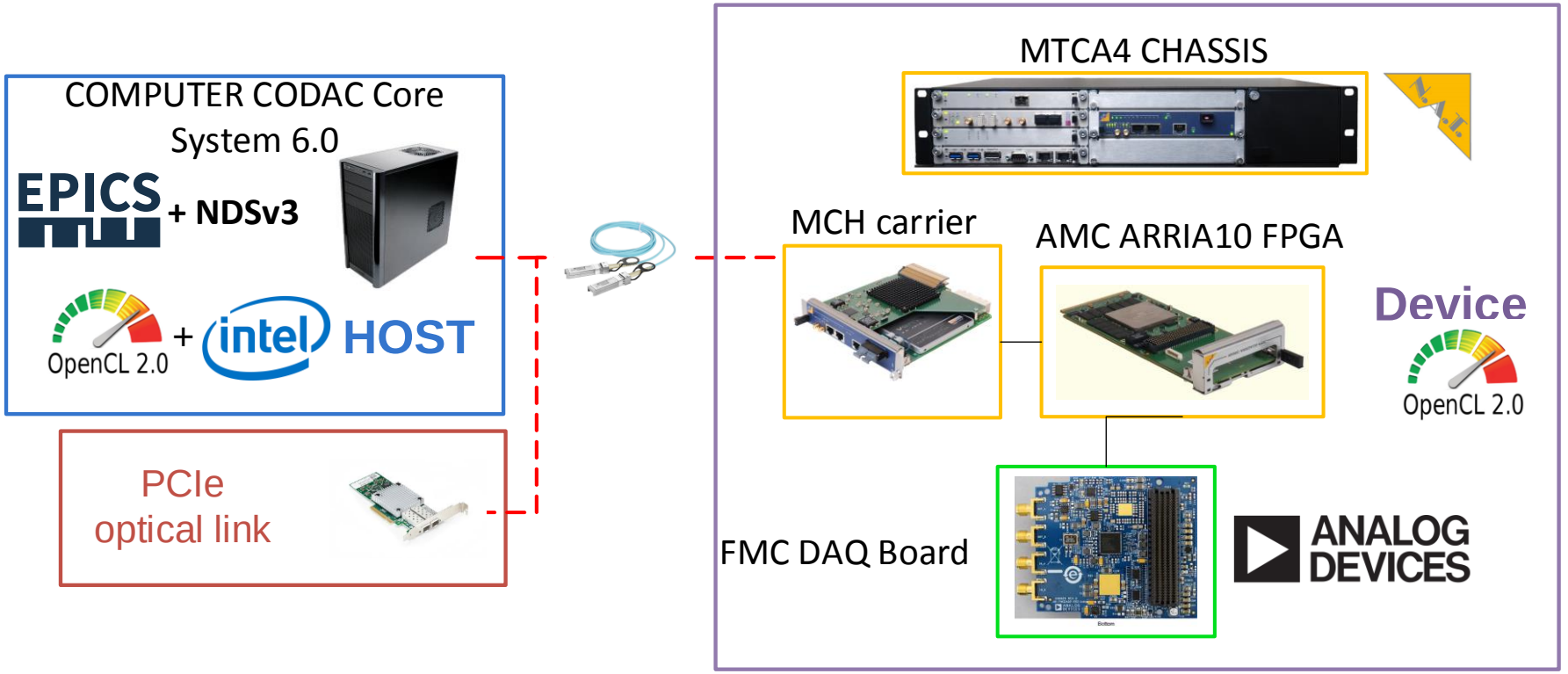
System Architecture: HW



- PC + PCIe + MTCA + AMC + (PROCESSING) + (I/O)
- **Thursay mini and poster on NDSv3!!**

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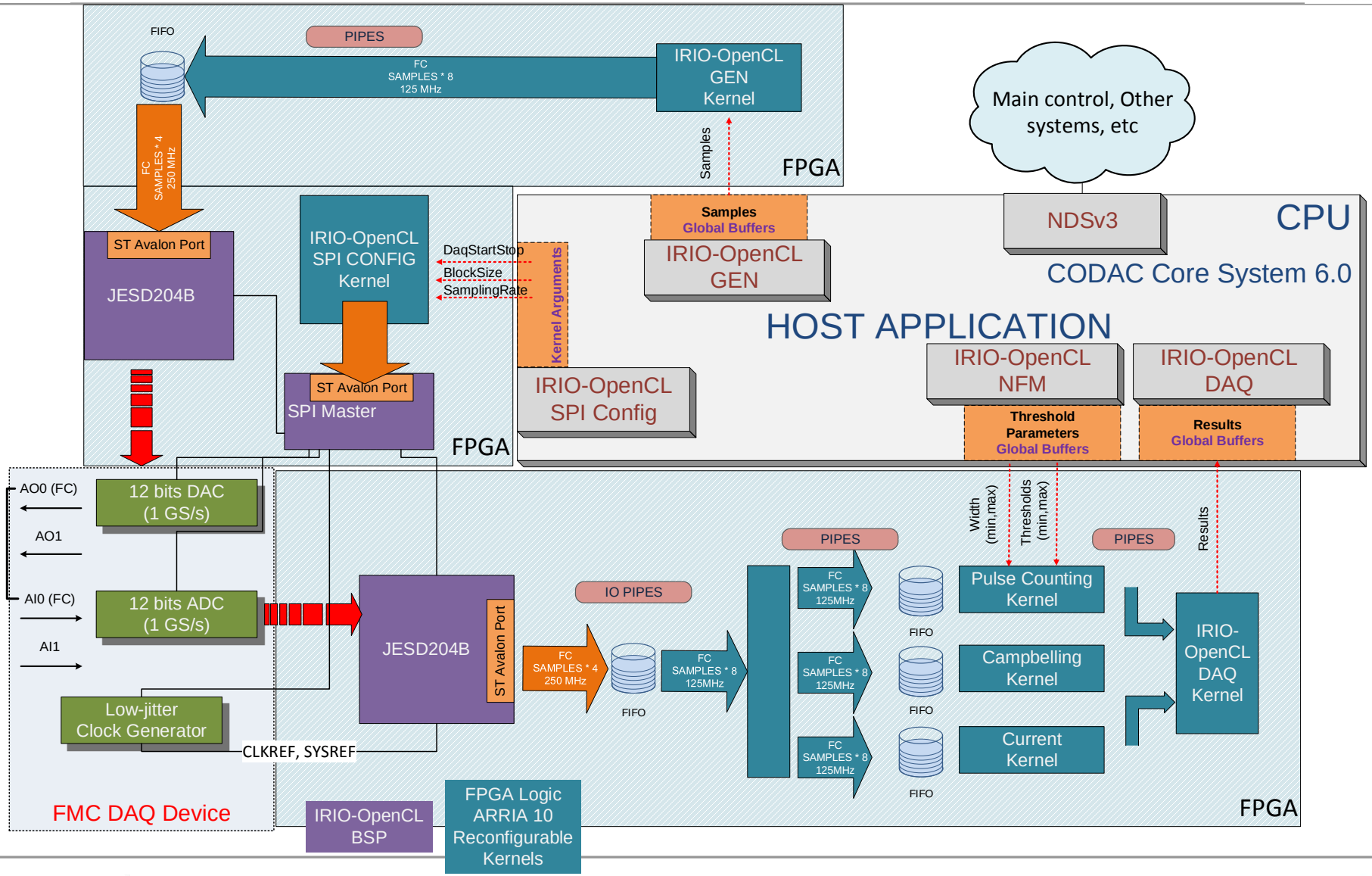
Implementation Overview



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Conclusions

- The Intel OpenCL compiler generates an efficient pipeline to process data at very high throughput. HW is described using OpenCL language.
- FPGA resource utilization with all the IRIO-OpenCL functionality is less than 50%.
- The hardware is managed using NDSv3 allowing an easy connection to EPICS.
- The complete platform is integrated in ITER CODAC Core System.
- **<u>Today's topic:</u> OpenCL is being extensively used for machine learning applications.**

More details in the plenary oral:

490. Methodology to standardize the development of FPGA-based intelligent DAQ and processing systems on heterogeneous platforms using OpenCL

<u>Thursday 9:00</u>

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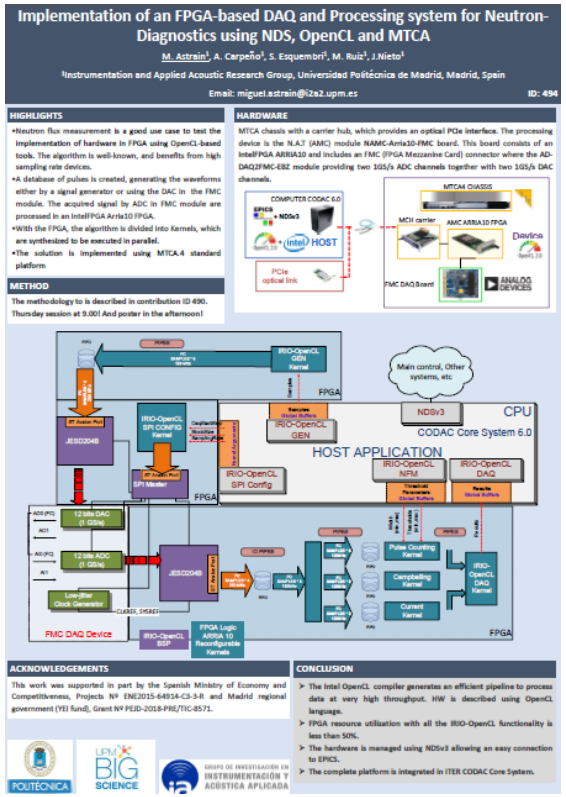

Thanks for your attention!!

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Poster location: P/2-4
15/05/2019