Max-Planck-Institut für Plasmaphysik

# Recent Diagnostic Developments with the ASDEX Upgrade Standard DAQ System using the FPGA implemented Serial I/O card „SIO2“

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# Outline

- The Serial DAQ Concept of SIO2 and its building blocks
- Coupled FPGAs for a Deterministic RT Data Transport
- New and Planned SIO2 Diagnostics at ASDEX Upgrade
- Summary

# Background of Today's Serial I/O concept

The challenge of experimental Data AcQuisition (DAQ) is always:

**Find a suitable solution to multiplex ADC channels into a computer!**

- many
- synchronized
- share data in real-time
- allow for modular hardware
- adaptable to fusion requirements

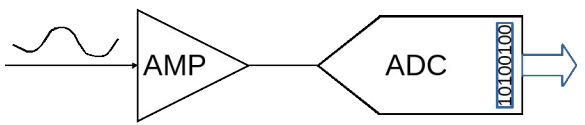
With 30 years of background ASDEX Upgrade's answer to this challenge is

**Pipeline periphery & 2nd generation Serial I/O computer interface.**

# One Channel: Amplifier, ADC, parallel out

A measuring channel cut down to the bare necessities

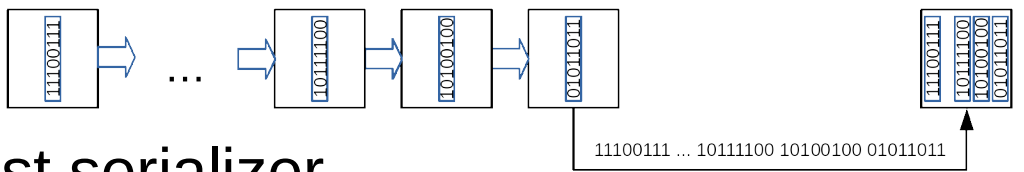
- easy and cheap to build in great numbers
- adaptable for signal conditioning and digital conversion
- configurable out of a virtual limitless electronics toolbox



# Multiplexer: Shift Register & Serializer

Combine a series of registers with a parallel shift logic

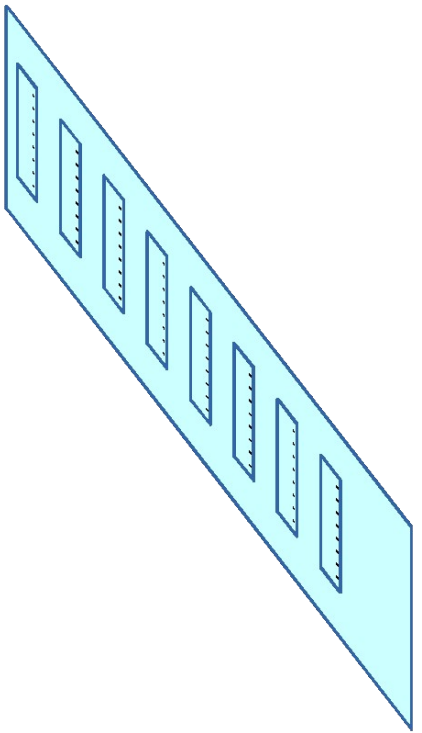
to bring a number of parallel data outputs into one row.




Shift all your data right into a fast serializer

to get a serial stream which can be transferred easily.

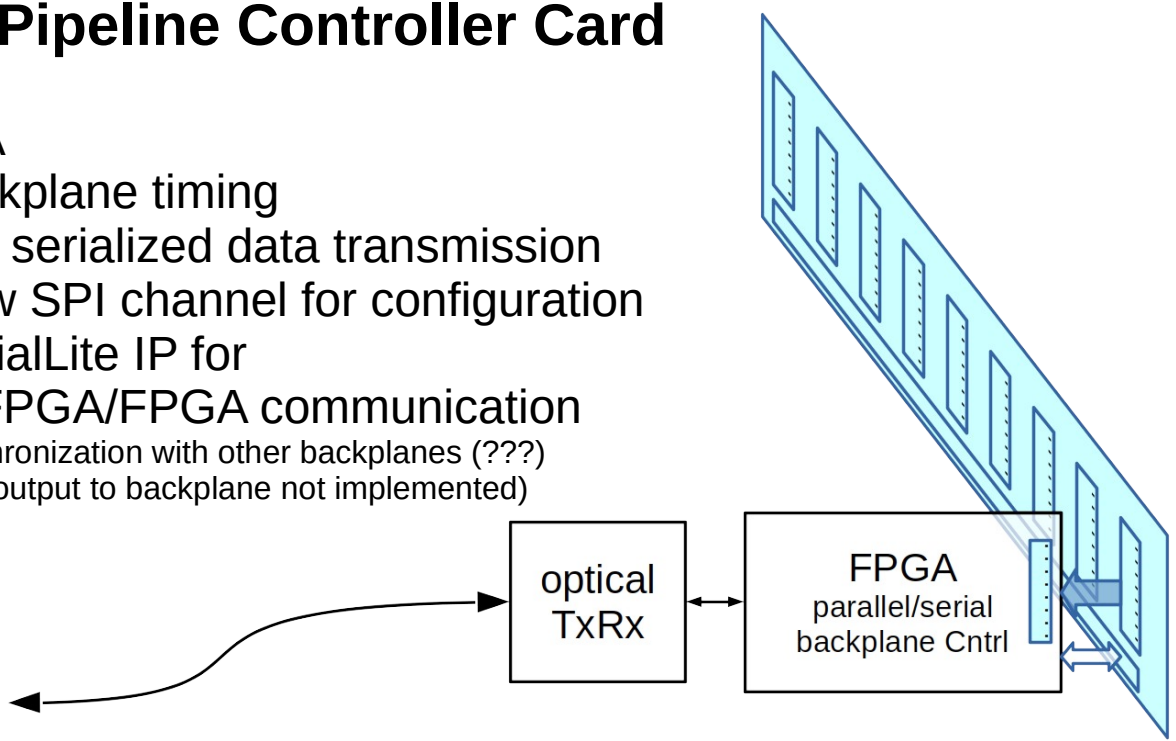
# Make it work => „Pipeline“ Backplane



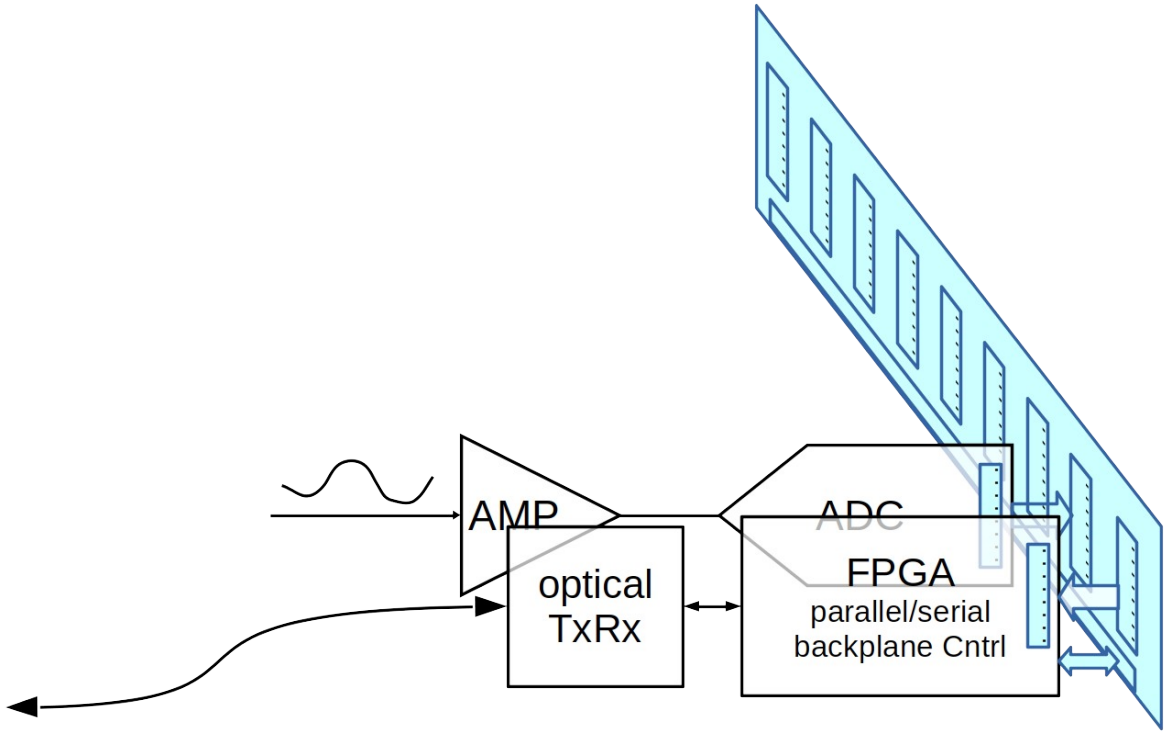
# Add Serializer to End of Pipeline

## The Pipeline Controller Card

FPGA
- backplane timing
- fast serialized data transmission
- slow SPI channel for configuration
- SerialLite IP for
  FPGA/FPGA communication
- synchronization with other backplanes (???)
- (fast output to backplane not implemented)



# Plug your „Modules“ into the „Pipeline“



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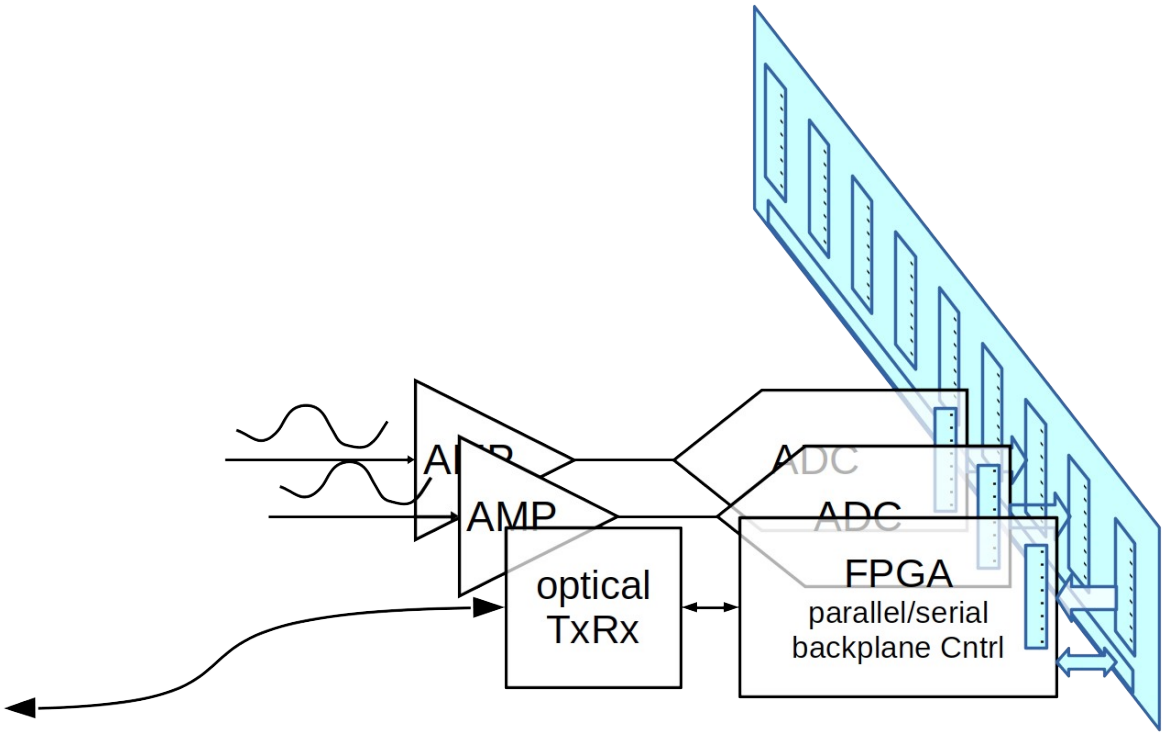

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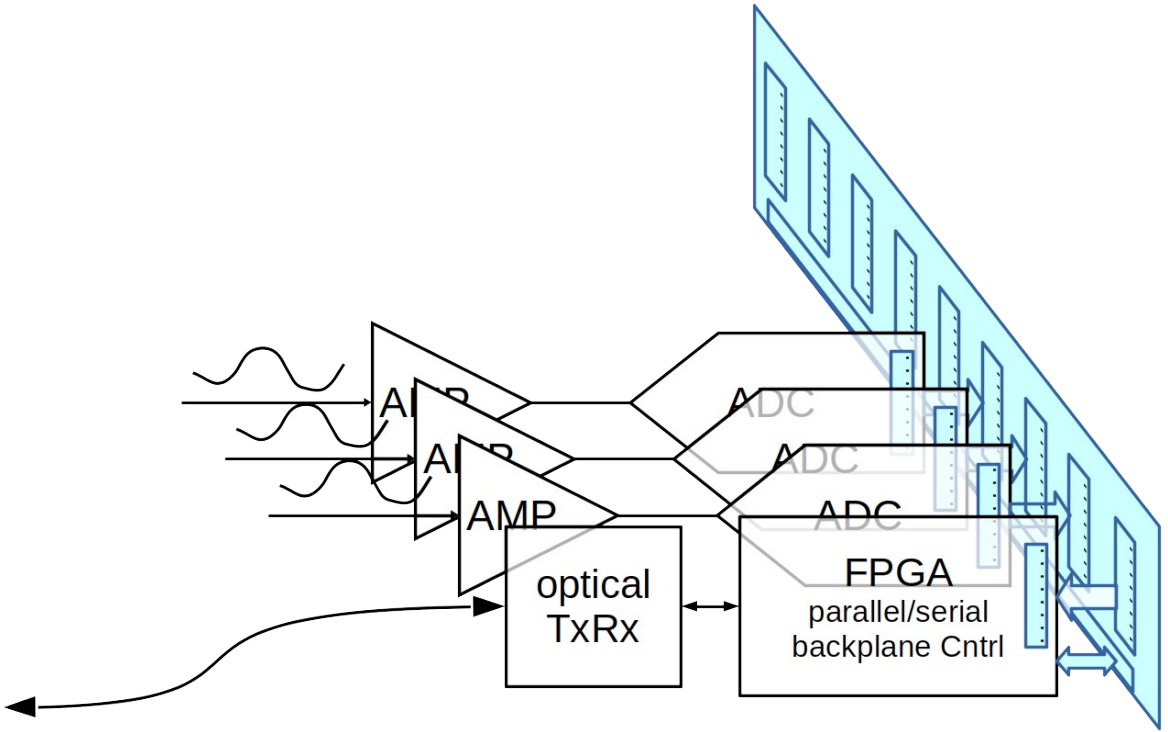

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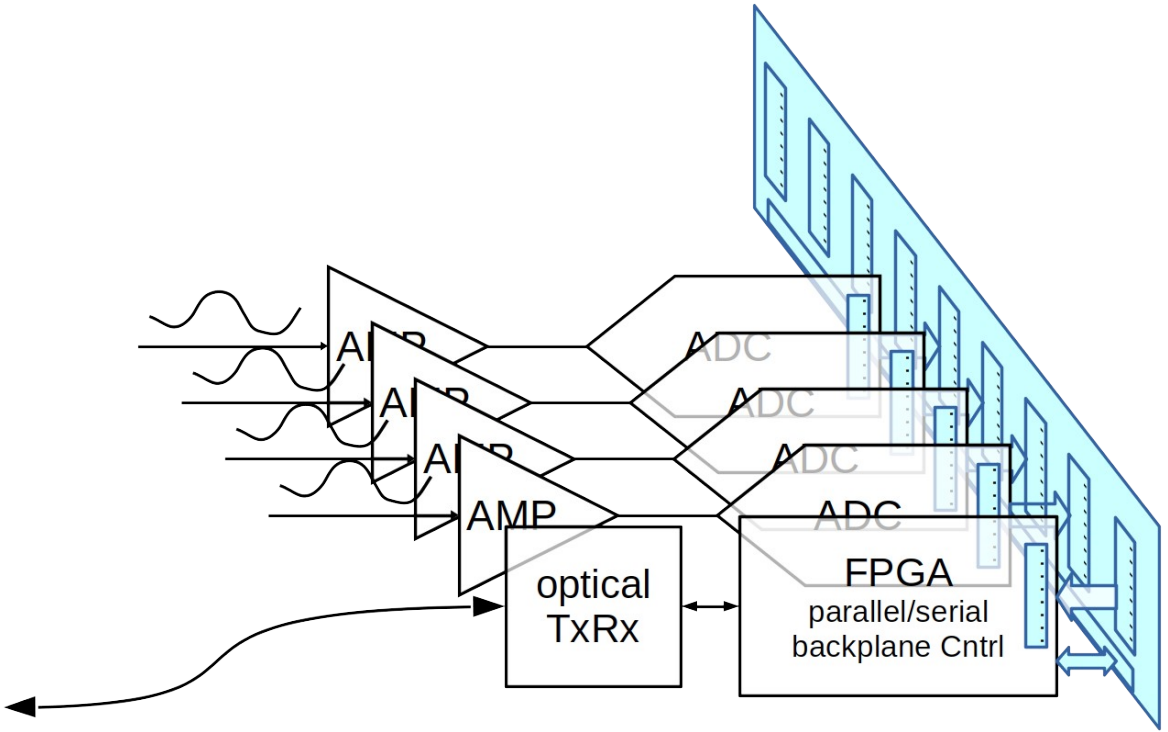

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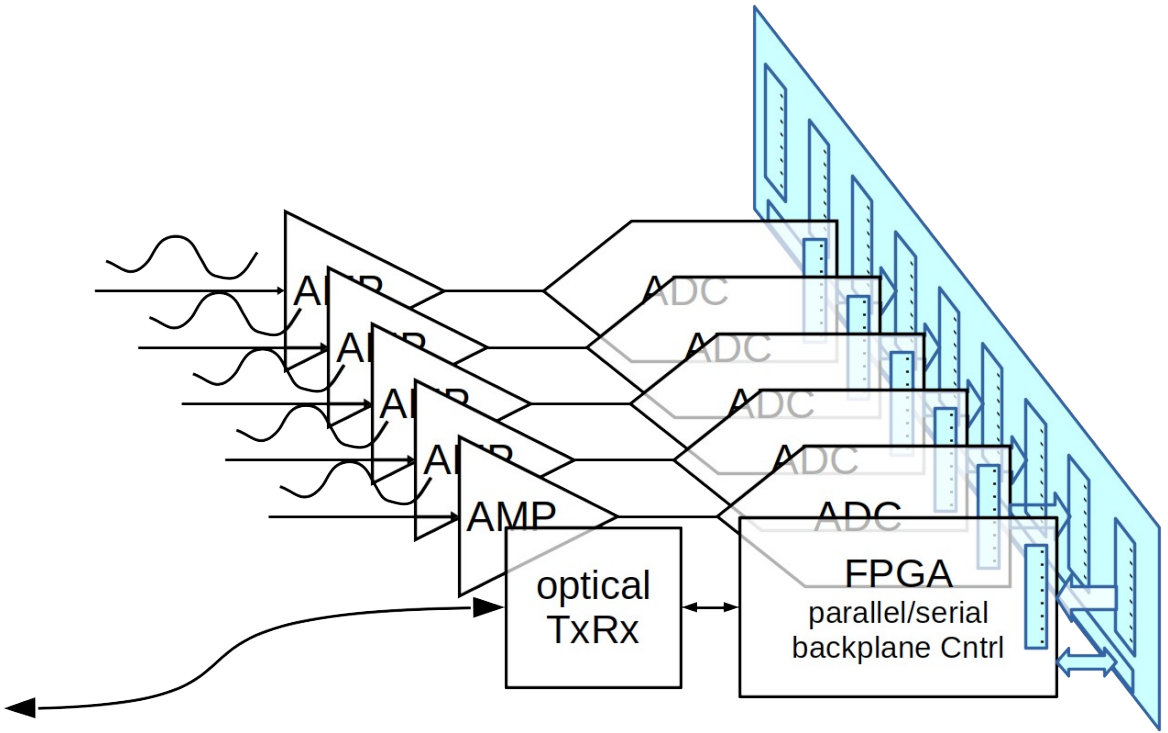

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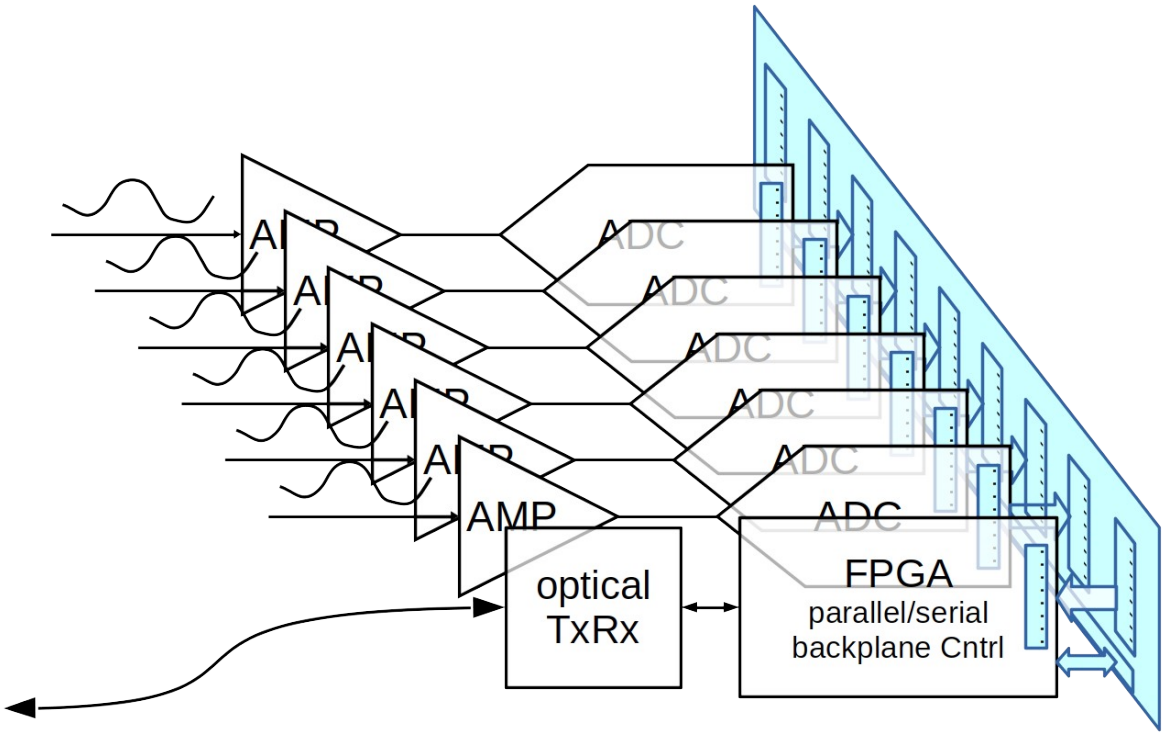

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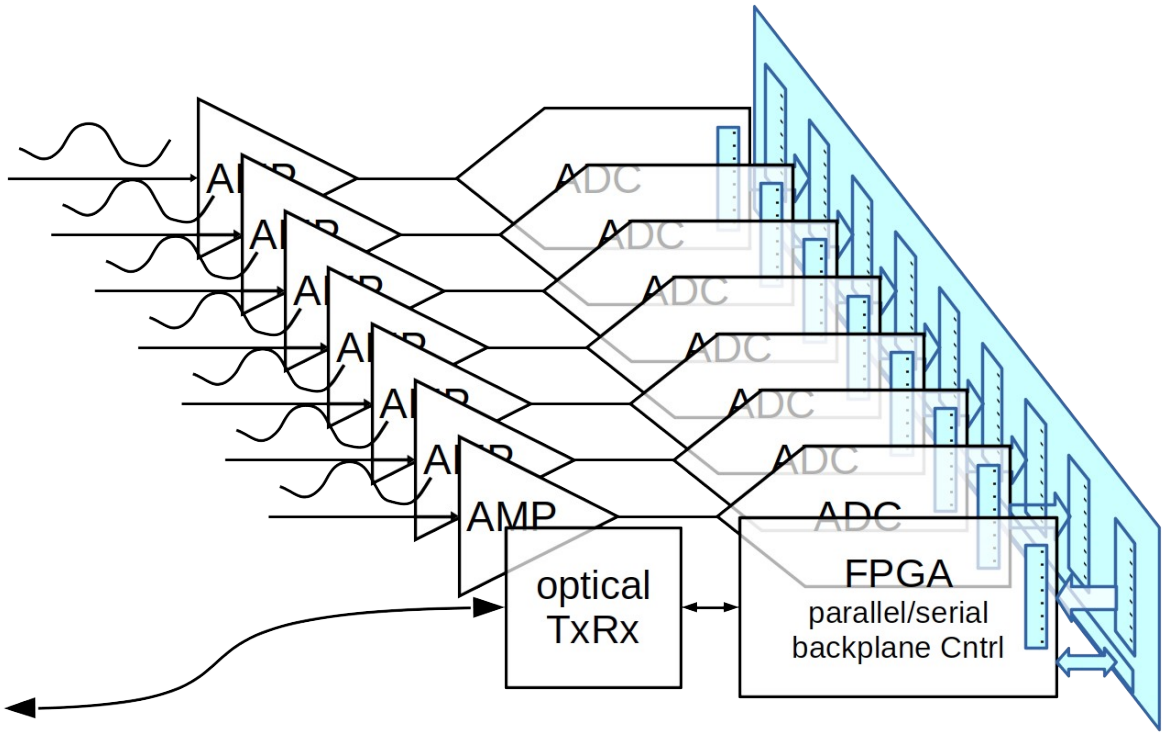

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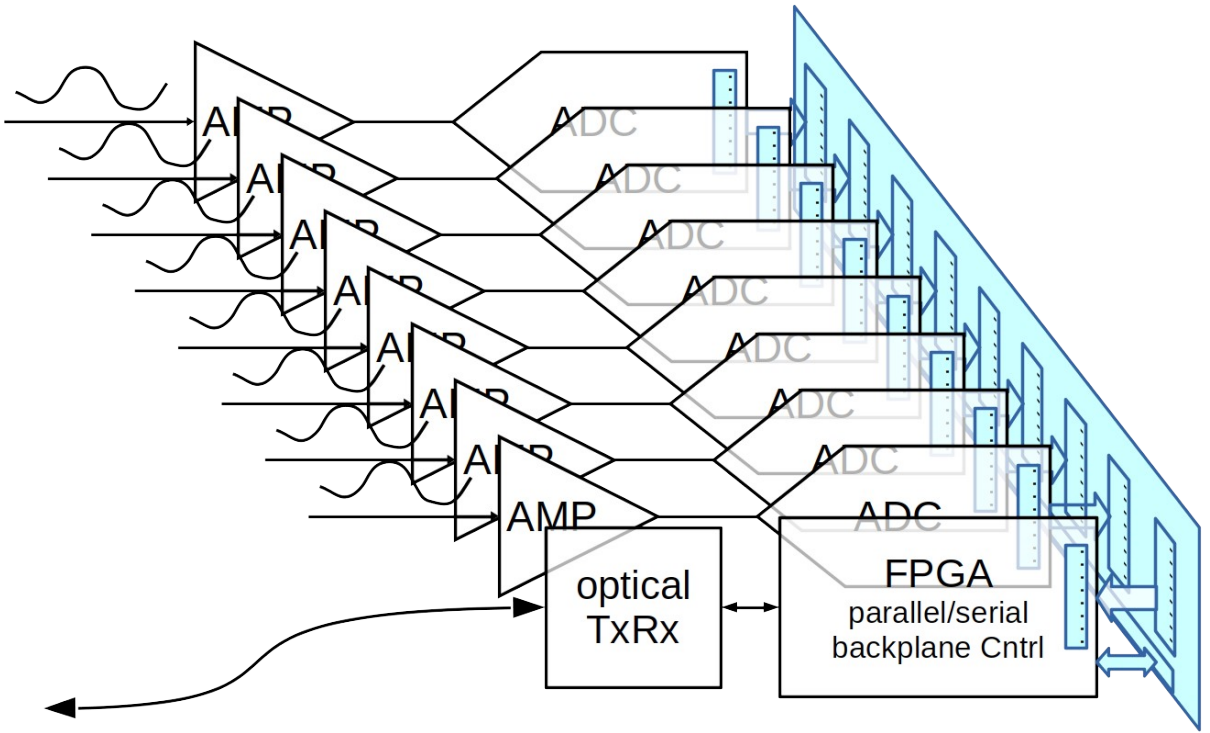
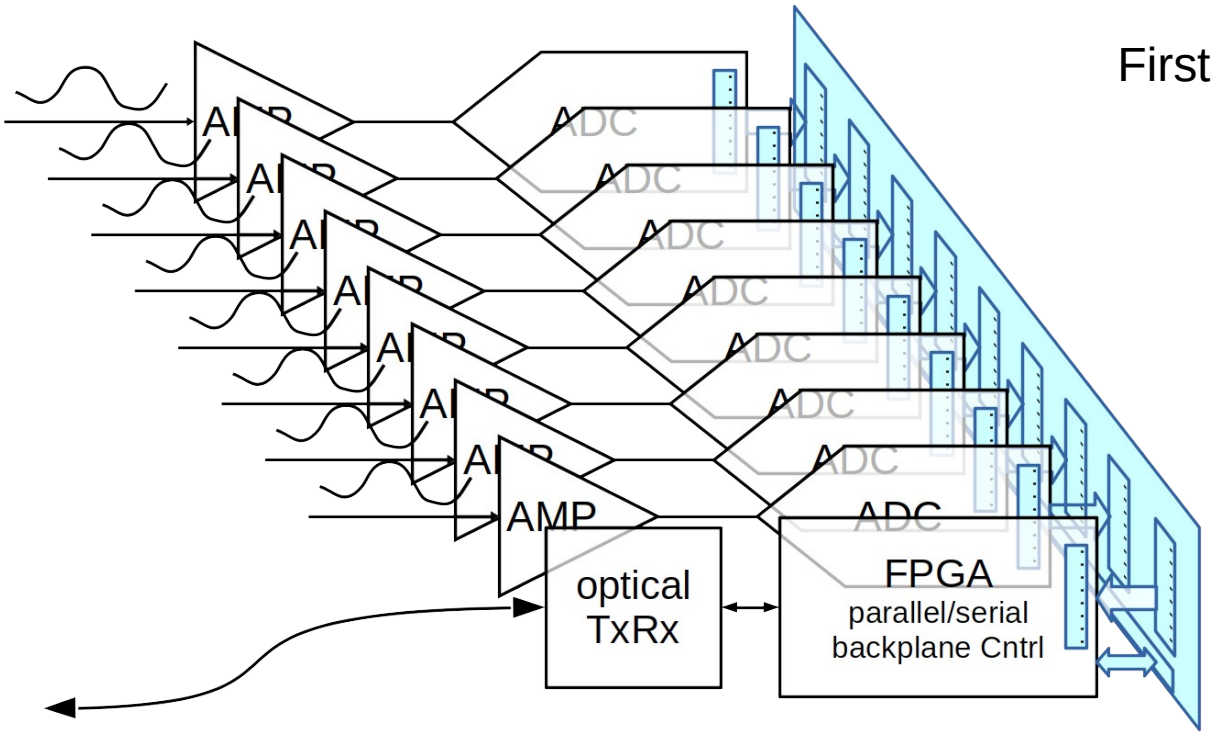


# How it works step by step



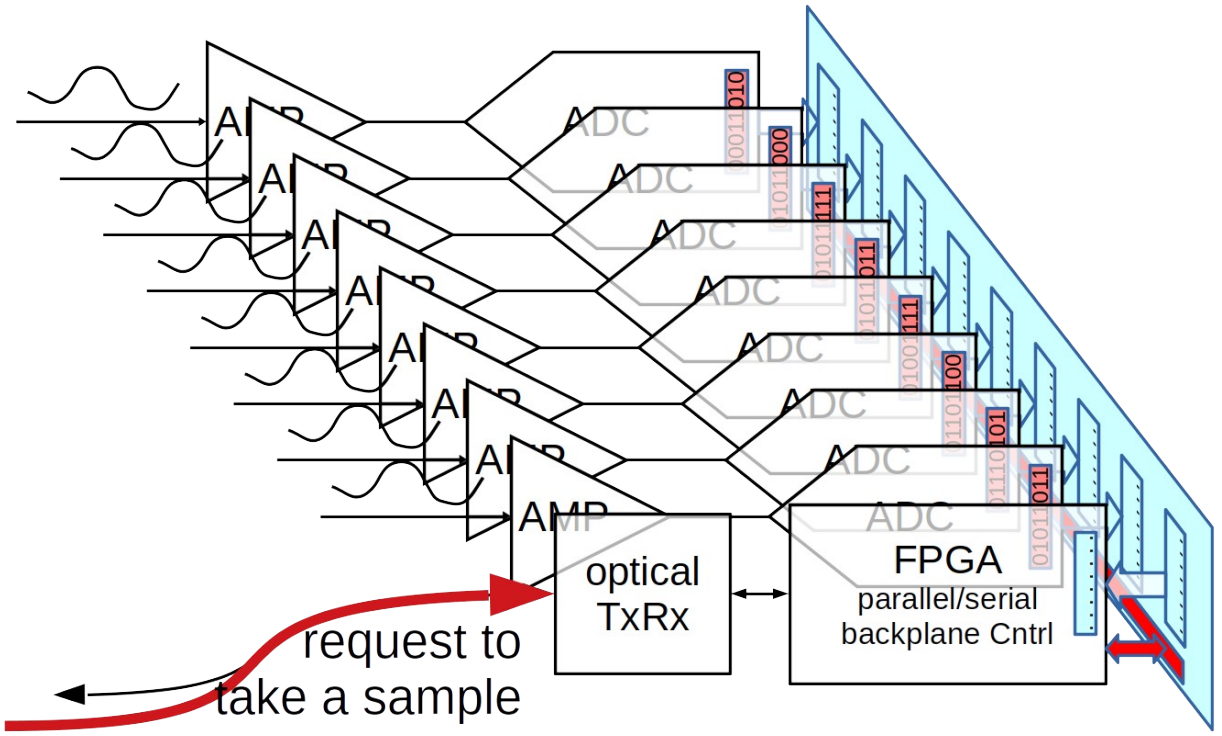

First step:

All modules receive a trigger clock pulse.

Trigger comes from the timing engine „above“.

(We'll see later what this means.)

# Sampling on Request from Above



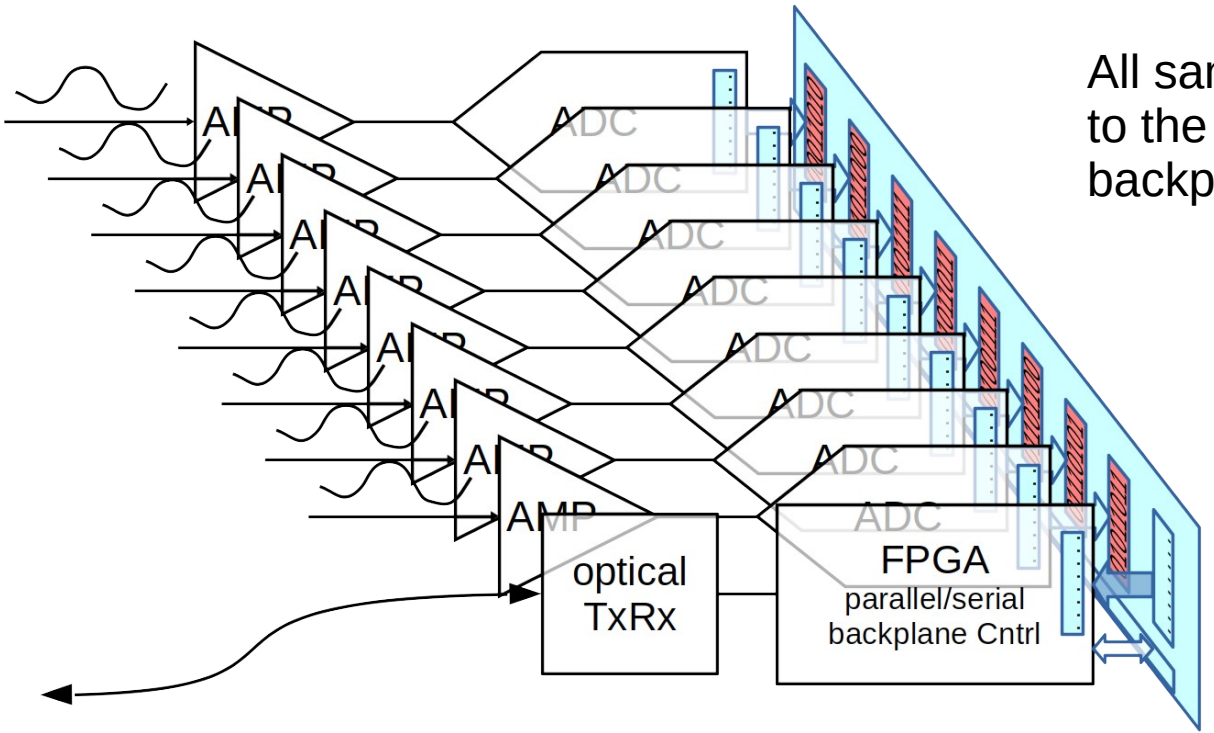

All modules receive a trigger clock pulse.

Trigger comes from the timing engine „above“.

(We'll see later what this means.)

All ADCs simultaneously produce a sample to the output register.

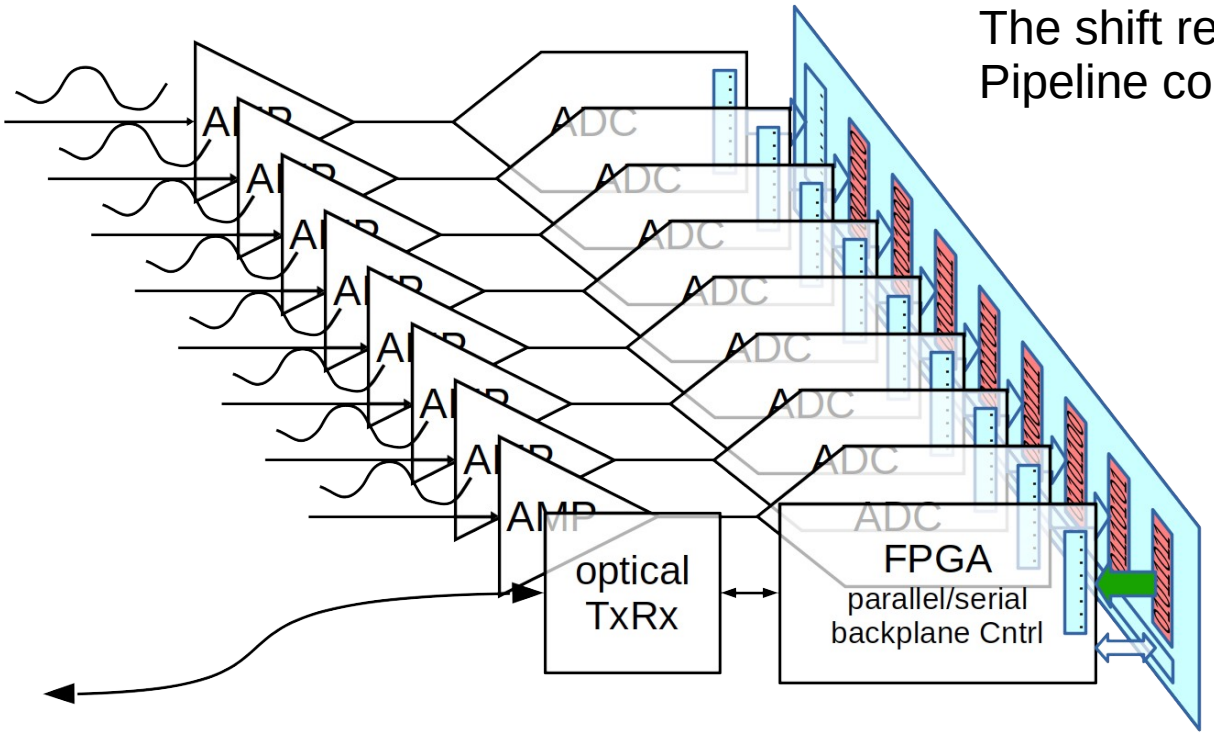
# Samples transferred onto the Pipeline




All samples are transferred to the corresponding backplane registers.

The backplane holds all acquired samples.

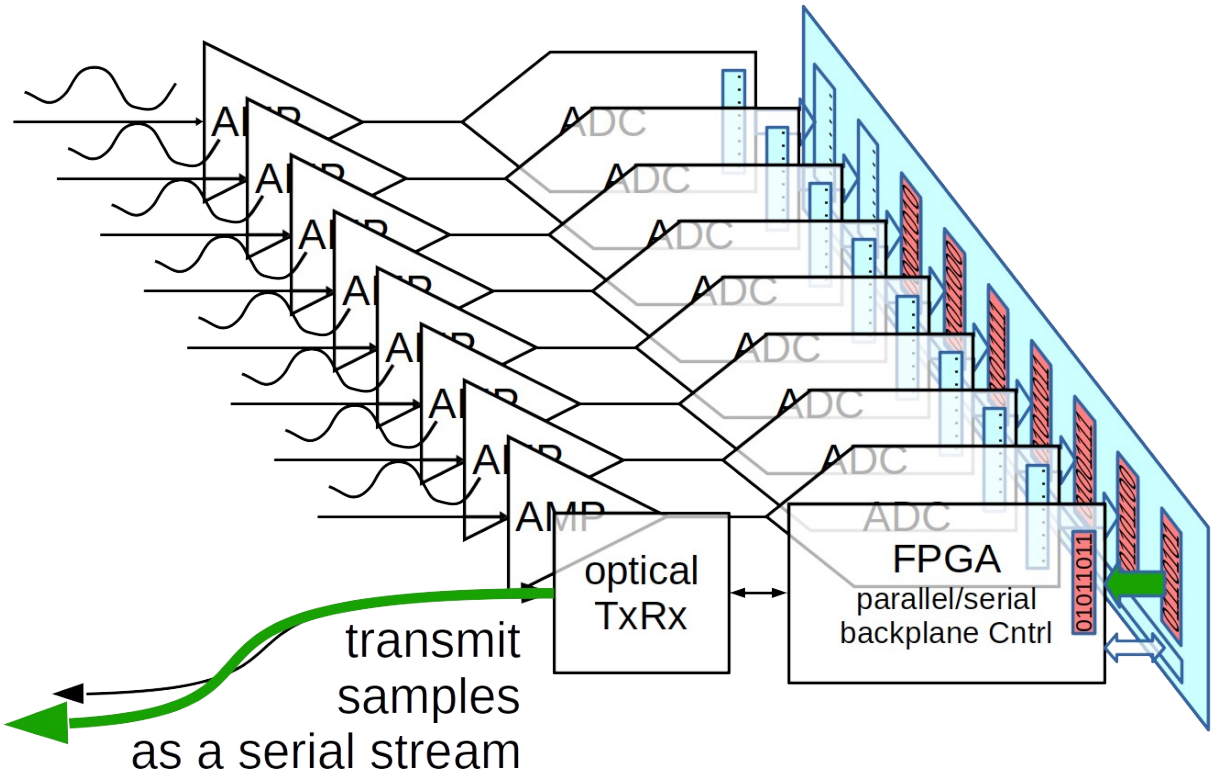
# Shifting samples along step by step




The shift register feature of the Pipeline comes into play ...

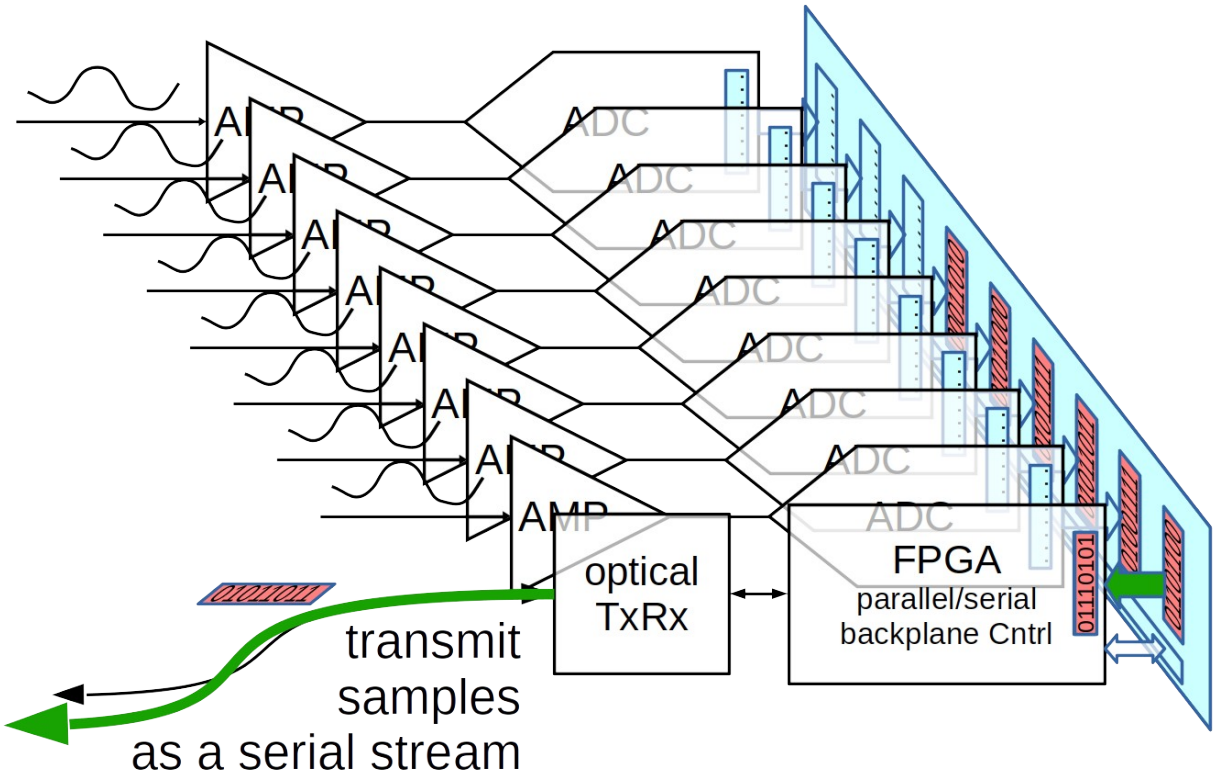
Samples move towards the parallel/serial converter and sender

# Shifting samples along step by step




Shift steps and backplane timing is conducted by the backplane controller.

# Shifting samples along step by step




The serial stream has only a few backplane clock steps latency.

# Things can be much more complex

I should say here: The shown sketches are simplified and abridged.

The system allows to set-up much complexer configurations:

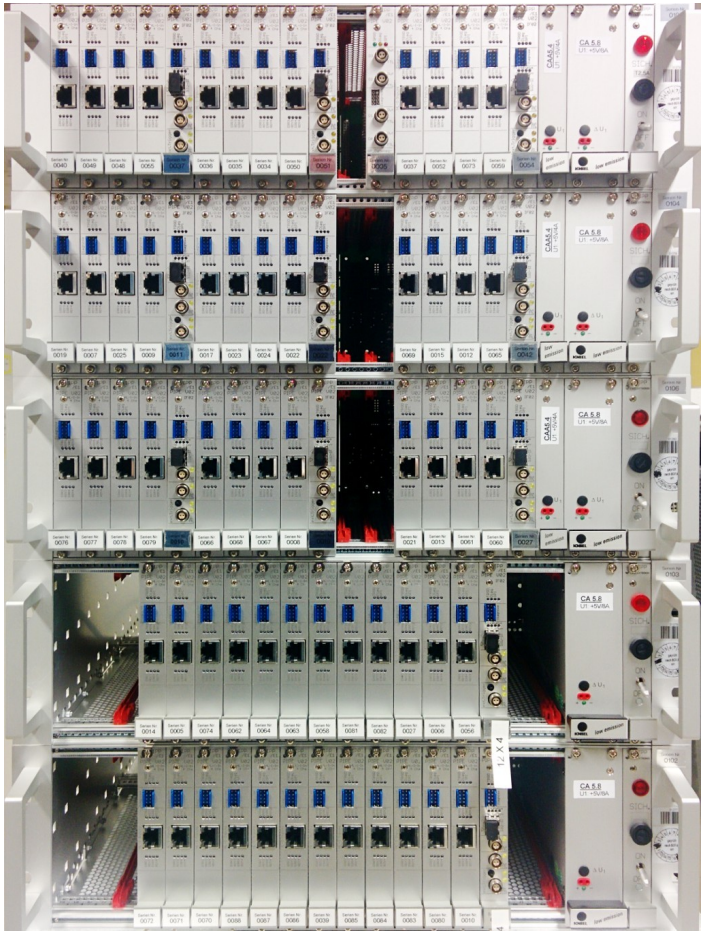
- Pipeline backplanes can be longer (up to 20 slots) or shorter (two slots)
- Analog inputs are adaptable to any kind of measurement requirement
- ADC-cards can be multi-channel (no limit, 2- or 4- channels are common)
- ADC-cards can have a high resolution time base to aquire time bursts (Required by diagnostics interested in resolving the pulse form of short events: Laser scattering, Reflectometry, Puls shape analysis.)

**All these variations have implications to be handled by the „higher logic“.**

# The Pipeline periphery of a real diagnostic

The new Soft-X-Ray Pipeline periphery provides 240 serial input ports for 240 twisted pair lines using standard TP-cables and RJ45 connectors

- 3 periphery crates host 48 channels each operated a 2 MHz sampling rate
  total data rate per crate: 96 MB/s
  - 3 Pipeline backplanes
    4 cards each
    4 ch./card
- 2 periphery crates host another 96 channels operated at 800 kHz sampling rate
  total data rate for both crates: 76 MB/s
  - 1 Pipeline backplane
    12 cards each
    4 ch./card



# Achievements – simple, modular, deterministic

- Simplified ADC / input channels
  - cut to the bare necessities (signal conditioning & ADC; digital receivers; event recording)
  - customizable to specific nuclear fusion diagnostics requirements
  - low costs per channel if produced in numbers
- Aggregation of multiple channels
  - condense multiple devices into multichannel Pipeline backplanes
  - synchronized operation of all channels within one Pipeline via the backplane
  - synchronize the operation of multiple Pipelines via the timing lockstep from the up-link FPGA
  - reduce uplink cabeling to one pair of optical fibres per Pipeline
    (get potential insulation in addition)
- **Deterministic time behavior**
  - From the moment the request-to-take-a-sample is sent to the Pipeline controller until the data stream arrives up-link the timing behavior of the whole periphery is deterministic.
  - It takes always the same number of FPGA clock ticks to sample, shift, serialize and send all data for that point in time up-link.

# „Up-Link“ Intelligence for Pipeline Periphery

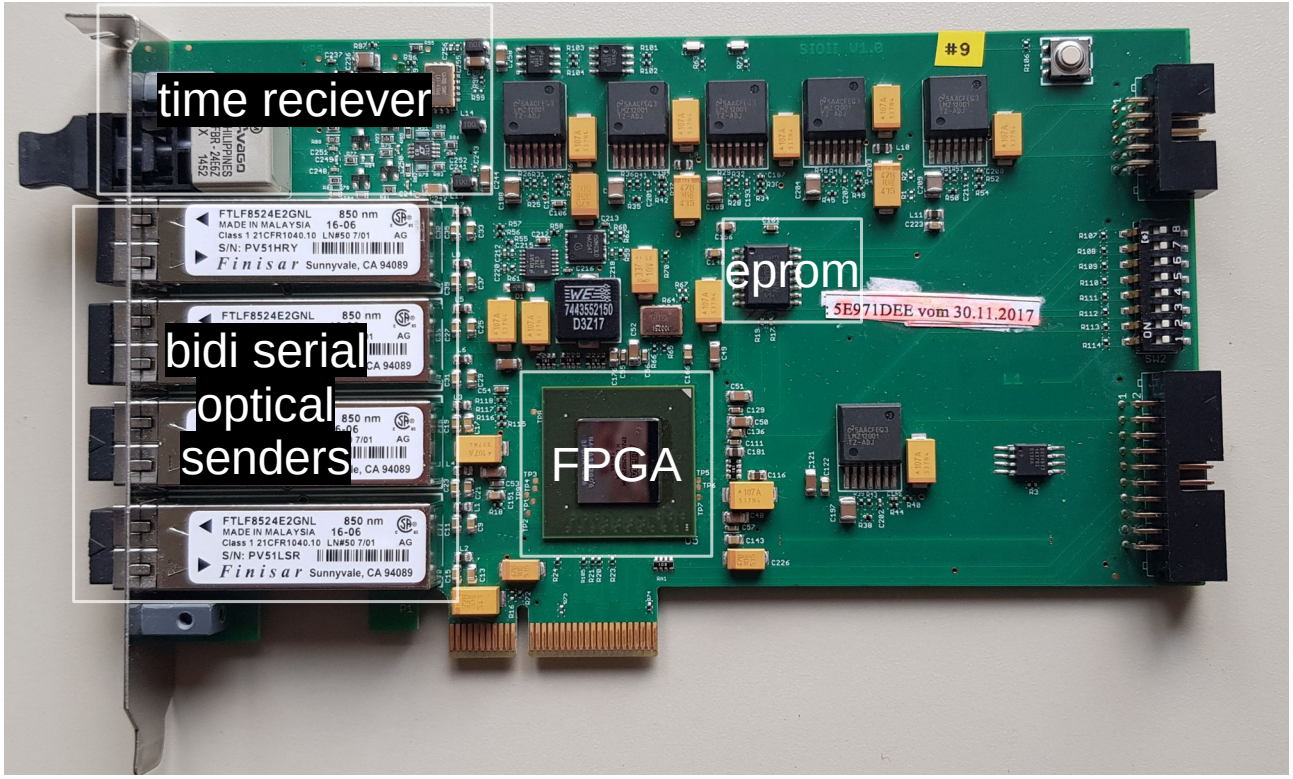
This concept for many ADC channels with a serial output
requires an up-link interface to a host computer to „manage“ the operation.

**SIO2** is an FPGA based PCIe card providing the necessary details to complement the Pipeline periphery to a fully featured DAQ system:

- the logic is implemented in an FPGA (Altera ARRIA II GX using the Quartus tools)
- four fast 2.5 Gbps SerialLite links to couple to down-link Pipeline FPGAs
- an extra optical fibre reciever for the central experiment clock signal
- a timing module implementing synchronized sampling timebase features (in FPGA logic)
  - time counter synchronization with the central experiment clock
  - timing and trigger generation for the periphery
  - storing time stamps to know when a DAQ transaction was started
- a PCIe computer interface (implemented as IP in the FPGA)
  with DMA capability to deliver data from the periphery directly into computer memory

# SIO2 basic function groups

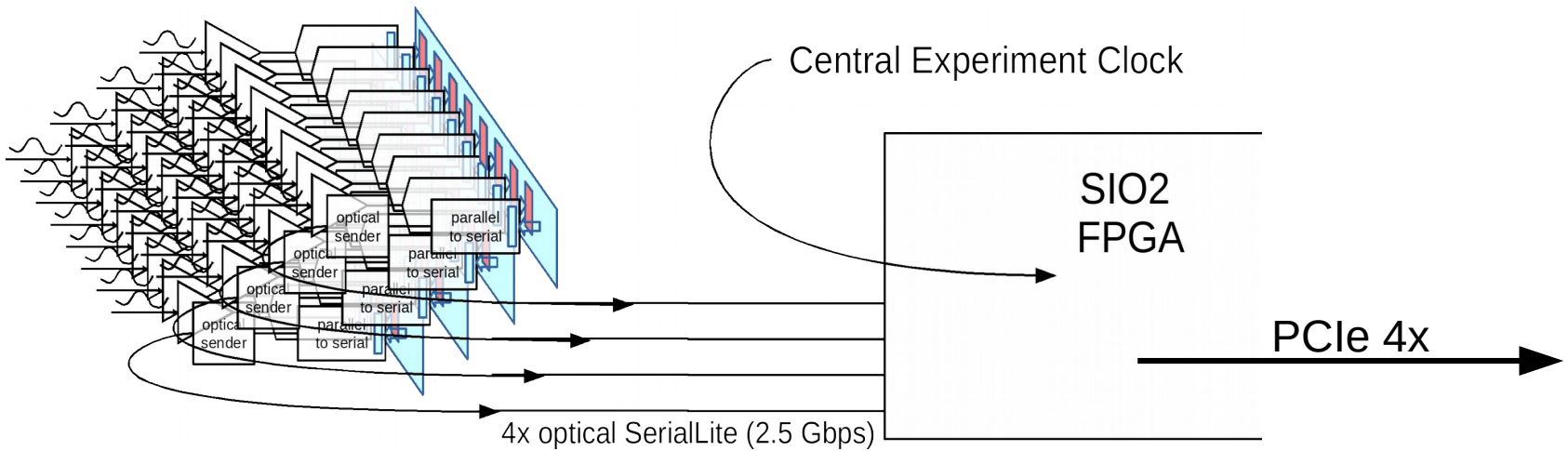
- time signal receiver
- 4x bidi optical senders
- FPGA (ARRIA II GX)
  - 125 MHz clock frequency
  - clock PLL derived from time
  - PCIe 4x Gen2 interface
- flash PROM
- programming socket
- test/extension socket
- multiple DC/DC supplies



# SIO2 Technology – FPGA, Optical Links, Time

**SIO2**, based on the serial link concept (used already earlier for ASDEX Upgrade) features completely new technology

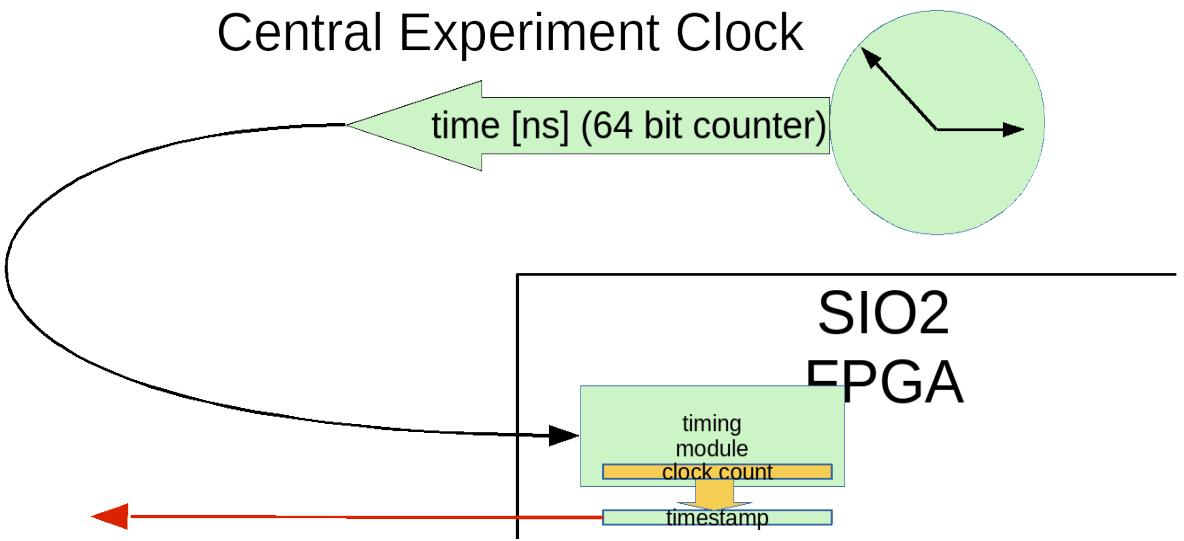
- complex logic goes into an FPGA
- four serial optical high speed connections connecting up to four Pipelines
- clock tick receiver for heart-beat synchronization with the experiment time
- 4x PCIe gen2 interface is implemented as IP being integral part of the FPGA



# Central Timing – a key feature of SIO

The Phase Locked Loop (PLL) coupling between SIO and the Experiment Clock is achieved via a fibre transmitting the 50 MHz heart beat and the clock count encoded with it.

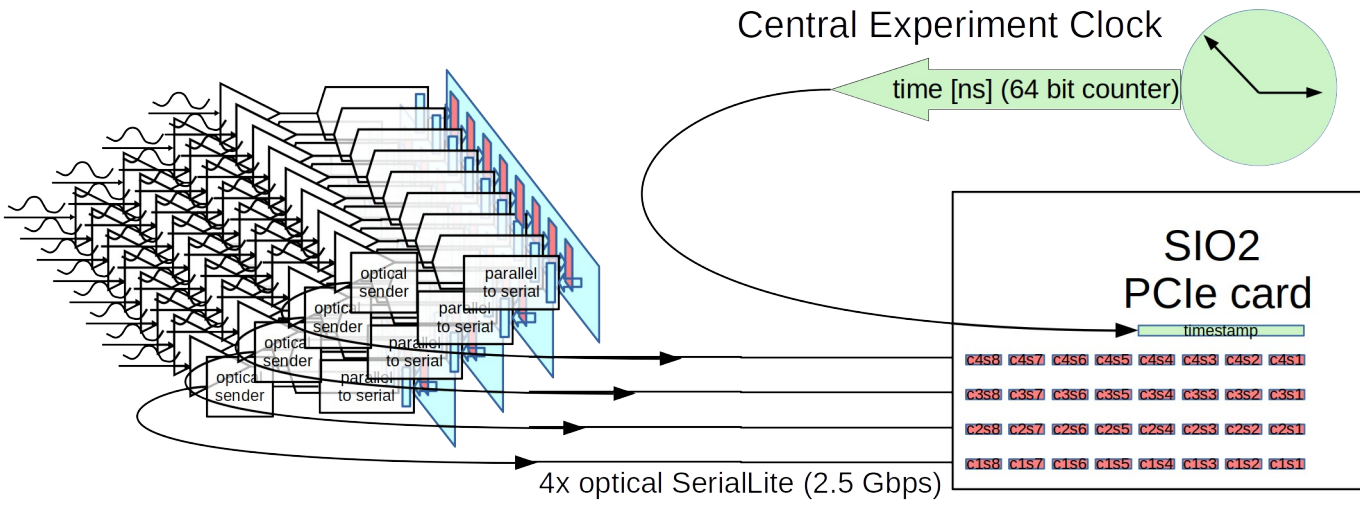
The SIO internal clock counter is synchronized with the central counter and the FPGA clock is directly derived from the PLL stabilzed central heart beat.



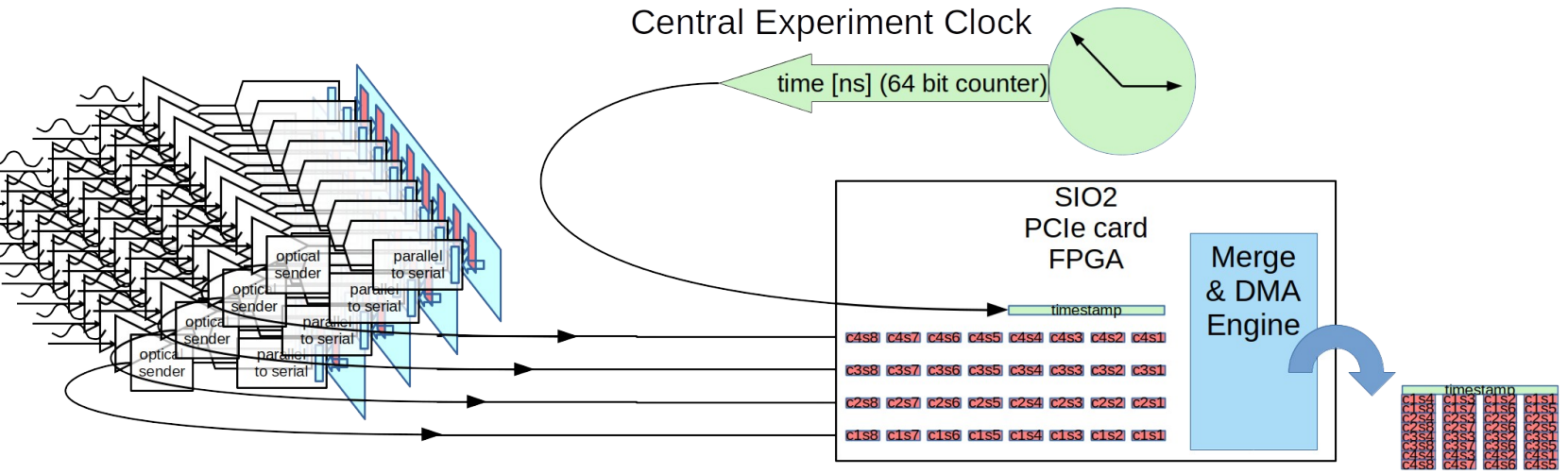

The timing module
following the clock count
is programmed
to generate trigger pulses
and store corresponding timestamps.

In fact
it generates the timebase
for the Pipeline periphery

# SIO2 always keeps together Time and Data



# Time and Data are merged into „Frames“



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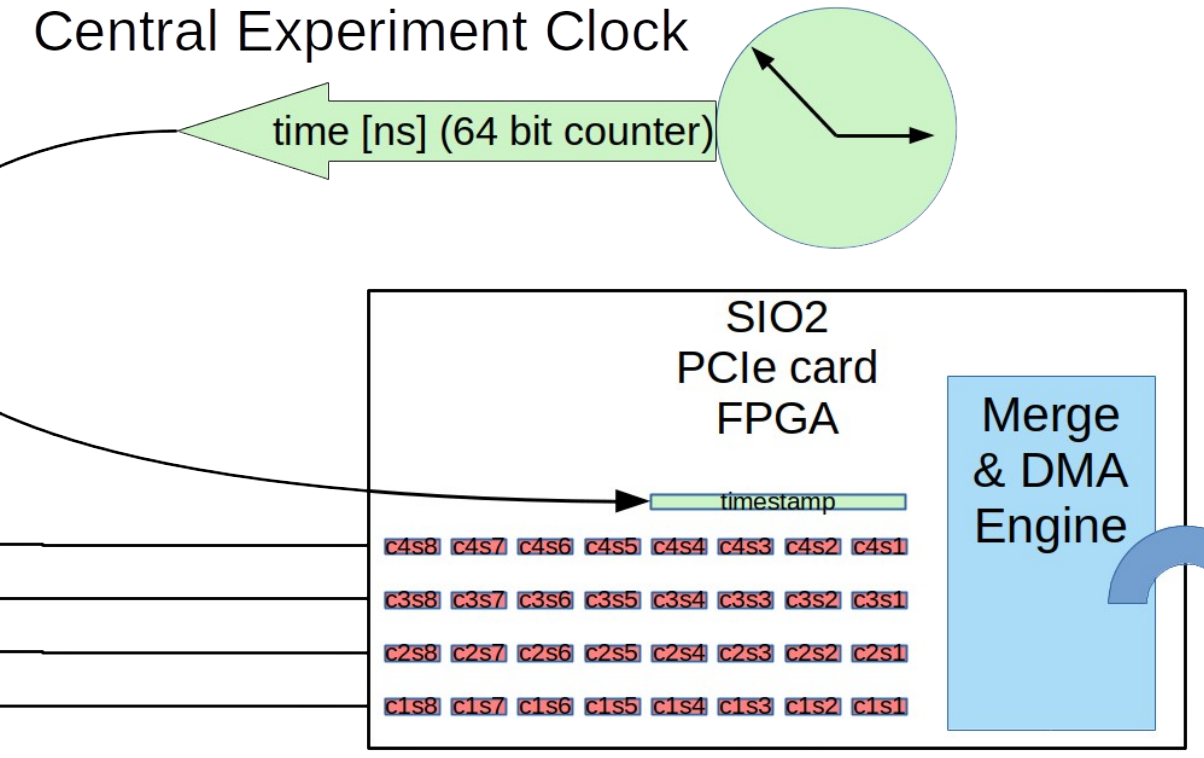



Frames are joined data blocks containing a timestamp as header and all samples taken at the same time as content.

Frames are transferred by the DMA logic of the SIO PCIe card filling a reserved shared computer memory.

RT processes can follow the data transfer progress and access measured samples with minimum latency.

# Default Timebases and beyond

The default operation mode for most DAQ systems is continuous sampling with a uniform sample rate over a predetermined time period.

This is still used for most diagnostics:

- SIO FPGA timing module maintains sampling rate for DAQ cycles over all channels in lockstep
- Each sample cycle generates a „frame“ consisting of time & samples
- Works up to a sampling frequency of 4 MHz
- Number of channels per Pipeline is limited by the bandwidth of backplanes and links

SIO2 now also supports external triggering to handle asynchronous events

- laser shots (used for Thomson scattering)
- stochastic events (hypothetic future applications)

The amount of data acquired with SIO2 during its real-time DAQ phase is limited only by the amount of preallocated host computer memory. (Which today may be tenth to hundreds of GiB.)

# Pipeline & SIO2 FPGAs - deterministic latency

- Pipeline Controller and SIO2 logic are both implemented with FPGAs
- AUG central experiment clock system is FPGA driven
- SIO2 FPGA clock frequency is PLL coupled to the experiment clock
- SIO2 & Pipeline FPGAs are heart-beat-coupled through serial links
- DAQ process of a SIO diagnostic runs completely deterministic locked to the clock frequency of the experiment
- SIO2 is able to operate on external triggers to acquire asynchronous events
- Every data trigger is time-stamped
- Every frame of sampled data contains its corresponding time stamp
- DMA transfer of data frames into pre-allocated contiguous memory provides a deterministic minimum latency for real-time data provision and access by subsequent analysis processes

# Actual SIO2 Diagnostics at ASDEX Upgrade

## Continuously sampling SIO2 diagnostics

- Soft-X-Ray Cameras (3 SIO2 cards, 48 ch., 2 MHz plus 1 SIO2 card, 96 ch., 800 Khz; total 364 MB/s)
- Mirnov Probes
- Divertor X-UV Emission diode arrays

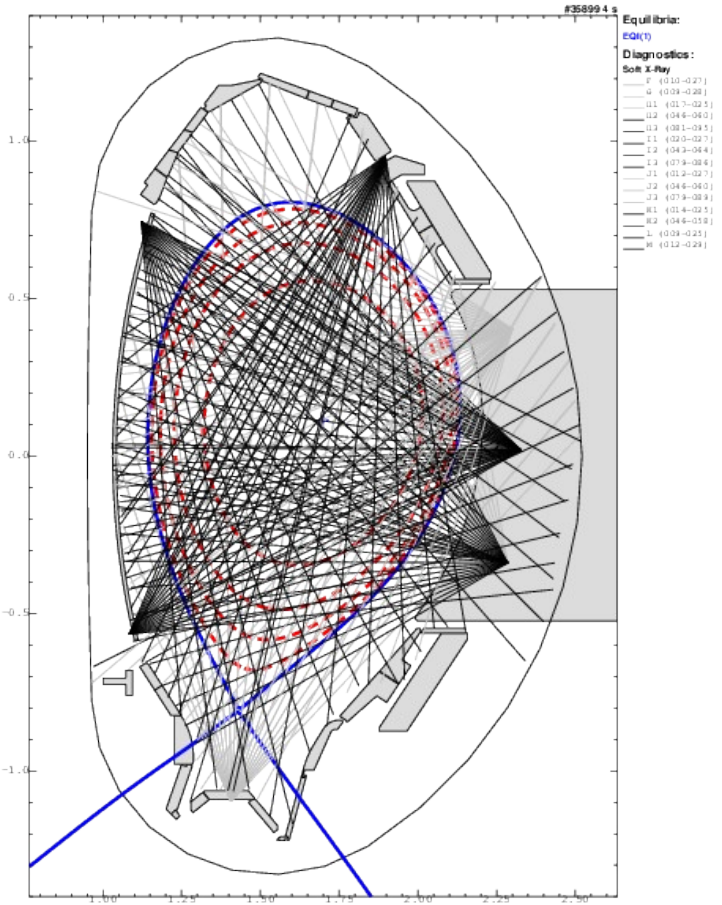
## Event triggered SIO2 diagnostics

- Divertor Thomson Scattering
  (134x 1 GHz channels, sample over 500 ns, burst rate of 20 Hz, total data rate 5.4 MB/s)
- Main Chamber Thomson Scattering (similar set-up, but 6 lasers allowing a repetition rate of 120 Hz)

- Requirements
- Discussed Solutions
- Reasons for SIO2
- Implementation Details

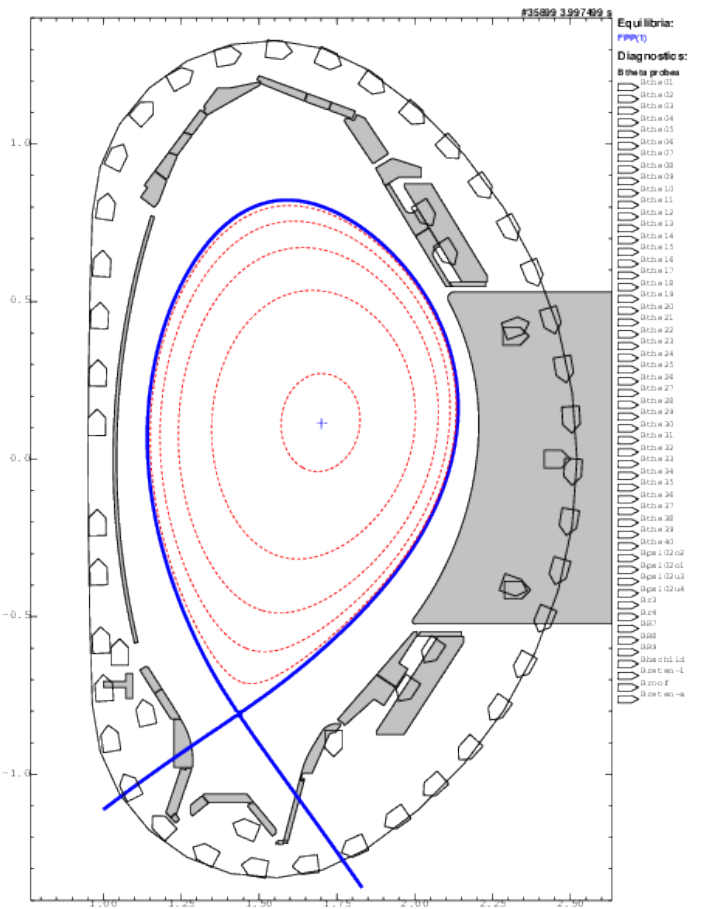
# Soft-X-Ray Cameras

- One of the initial Transputer diagnostics
- 2nd refurbishment since then
- Renewal and consolidation of hostsystem
- RT integration with Control required
- Ported from Solaris to RT-enabled CentOS7
- Adaptation of HOTLink to SIO periphery
  - 3x16 HOTLink channels aggregate into one SIO2 using 3 links
  - 144 Soft-X-Ray channels employ 3 SIO2 cards
  - 96 slower channels connect to a 4th SIO2 card
  - one x86-64 Linux system (Fujitsu RX2540, 2 sockets, 64 GiB)
  - RT transfer via DMA into Linux reserved memory at about 4x 100 MiB/s



# Mirnov Probes

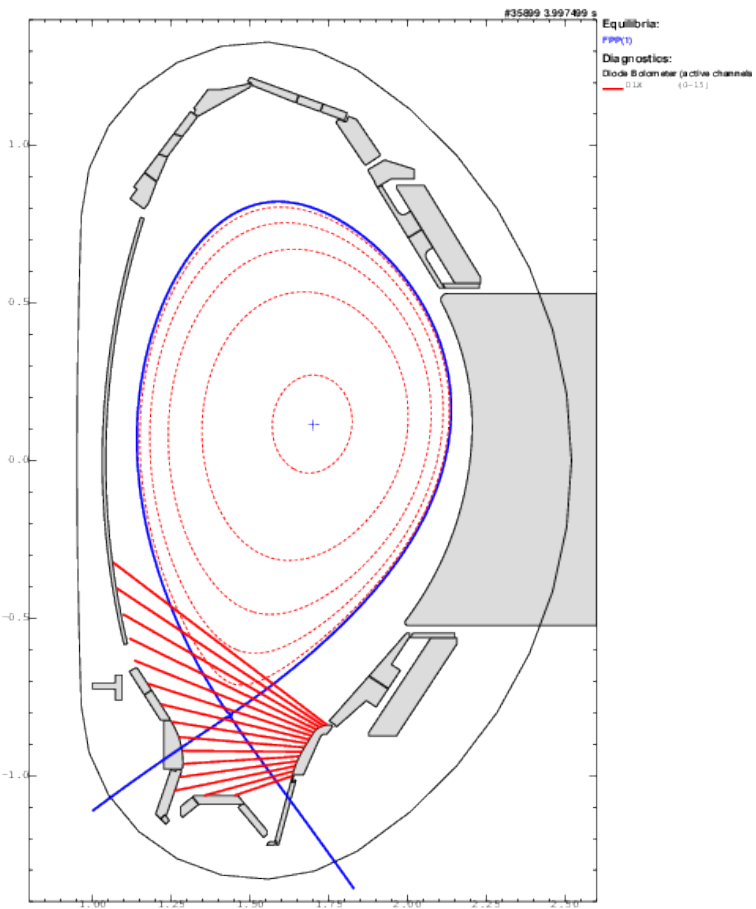
- One of the initial Transputer diagnostics
- 2nd refurbishment since then
- Similarities with Soft-X-Ray: HOTLink
  - Adaptation of HOTLink to SIO periphery
- Renewal and consolidation of hostsystem
- RT integration with Control required
- Ported from Solaris to RT-enabled CentOS7




**Poster O/8-3**

# Divertor X-UV Emission Diodes

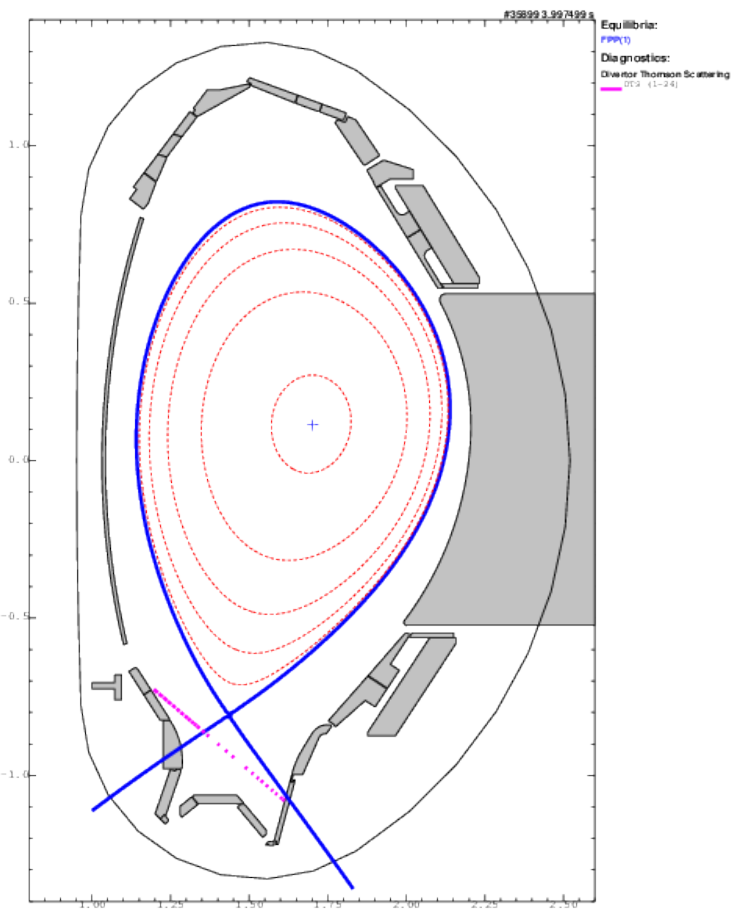
- RT enabling of 16 X-UV channels in the Divertor region
- Existing Pipeline & SIO1 channels separated into a new SIO2 diagnostic
- Real-time enabled CentOS 7 environment
- Real-time Discharge Control Application (DCS-AP) running parallel to DAQ




**Poster O/8-3**

# Divertor Thomson Scattering

- Neodym-Yag Laser crossing the Divertor area
- 26 scattering volumina observed by
  5 spectral channels each
  130 1GHz signals (+ 4 monitor signals)
- Very reasonable data amount
  268 KB per scattering event
  20 Hz event rate deliveres 5.36 MB/s
  64 MB per 12 s plasma discharge




**Poster O/8-3**

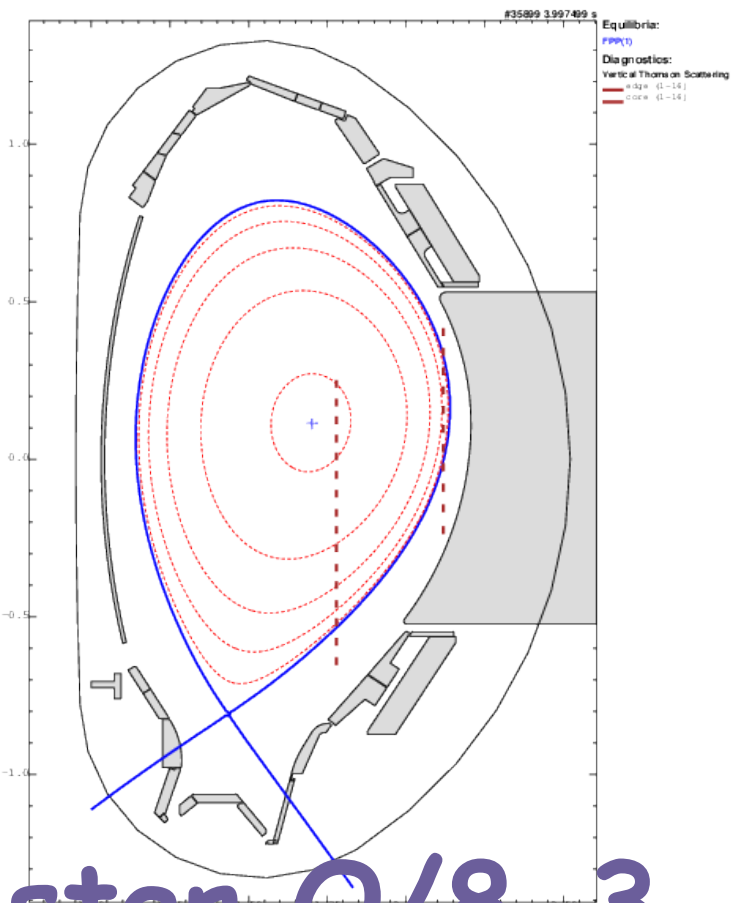
# 1 GHz ADC channels for Thomson Scattering

- 1 GHz sampling for 1 µs (scattering event) every 50 ms (Laser rate 20 Hz)
- External DAQ posttrigger from Laser pulse (adapts for a slight Laser jitter)
- A build to purpose ADC using Pipeline/SIO2 concept was preferred over an expensive purchase of a commercial 1GHz DAQ system
- The ADC development took about two years.
- SIO2 FPGA implementation of external trigger capability took about 3-6 month
- Implementation details:
  - Pipeline ADC card implements a high bandwidth preamplifier and a free running 2 channel 1GHz, 14bit AD9691 ADC delivering via JESD204B protocol eight (8) serial streams into an ARRIA V FPGA implementing an appropriate FIFO structure
  - FPGA memory is good to cache 32 KiB for each scattering event
  - The ADC card operates externally triggered and completely autonomous for a single laser scattering event
  - Between scattering events is plenty of time to transfer data up-link to host computer via SIO2

Poster O/8-3

# Main Chamber/ Edge Thomson Scattering

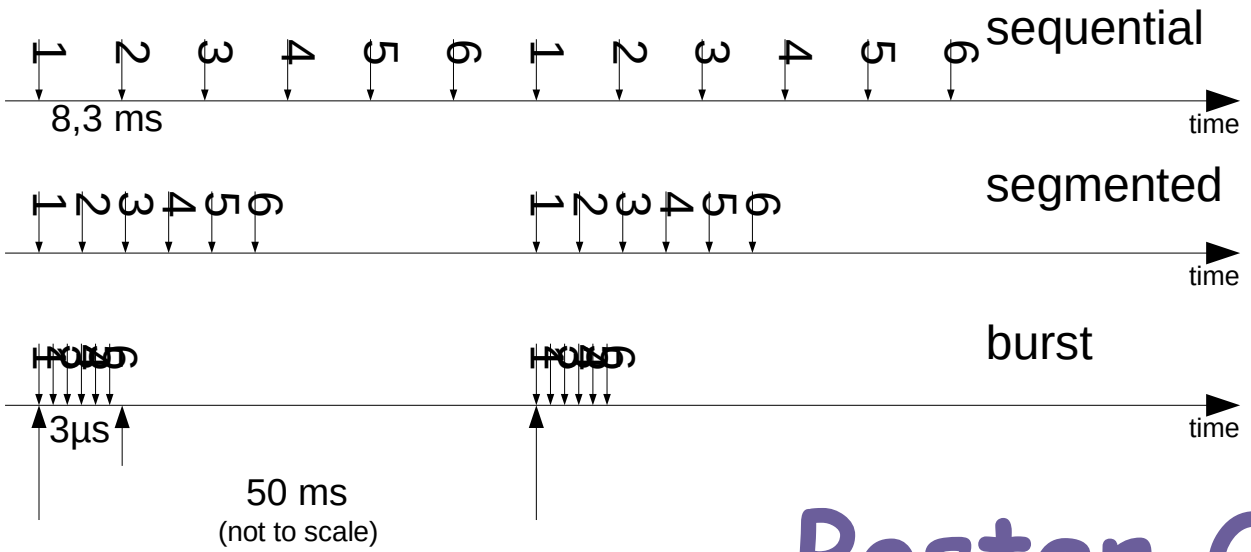
- 6 Neodym-YAG lasers crossing core or edge plasma
  - 16 scattering volumina observed
  - legacy observation/detection hardware in place
  - 20 Hz repetition rate per laser
  - 120 Hz repetition rate of scattering events
- Requirements for operating six lasers
  - criterion to differentiate lasers is required
  - variable laser timing desired (sequential, segmented, burst)
- Reason for touching a running Diagnostic:
  - RT Linux required to integrate with DCS
  - Replace outdated host computer hardware
- Reason for Pipeline & SIO2:
  - replacement & cosolidation of Acquiris channels
  - see Divertor TS, development mostly done




Poster O/8-3

# Possible timing modes with six lasers

- Sequential mode allows the read-out of 1GHz ADC periphery between laser pulses
- Segmented mode may run into time constraints for data read-out
- Burst mode requires to cache six laser shots and allow delayed read-out

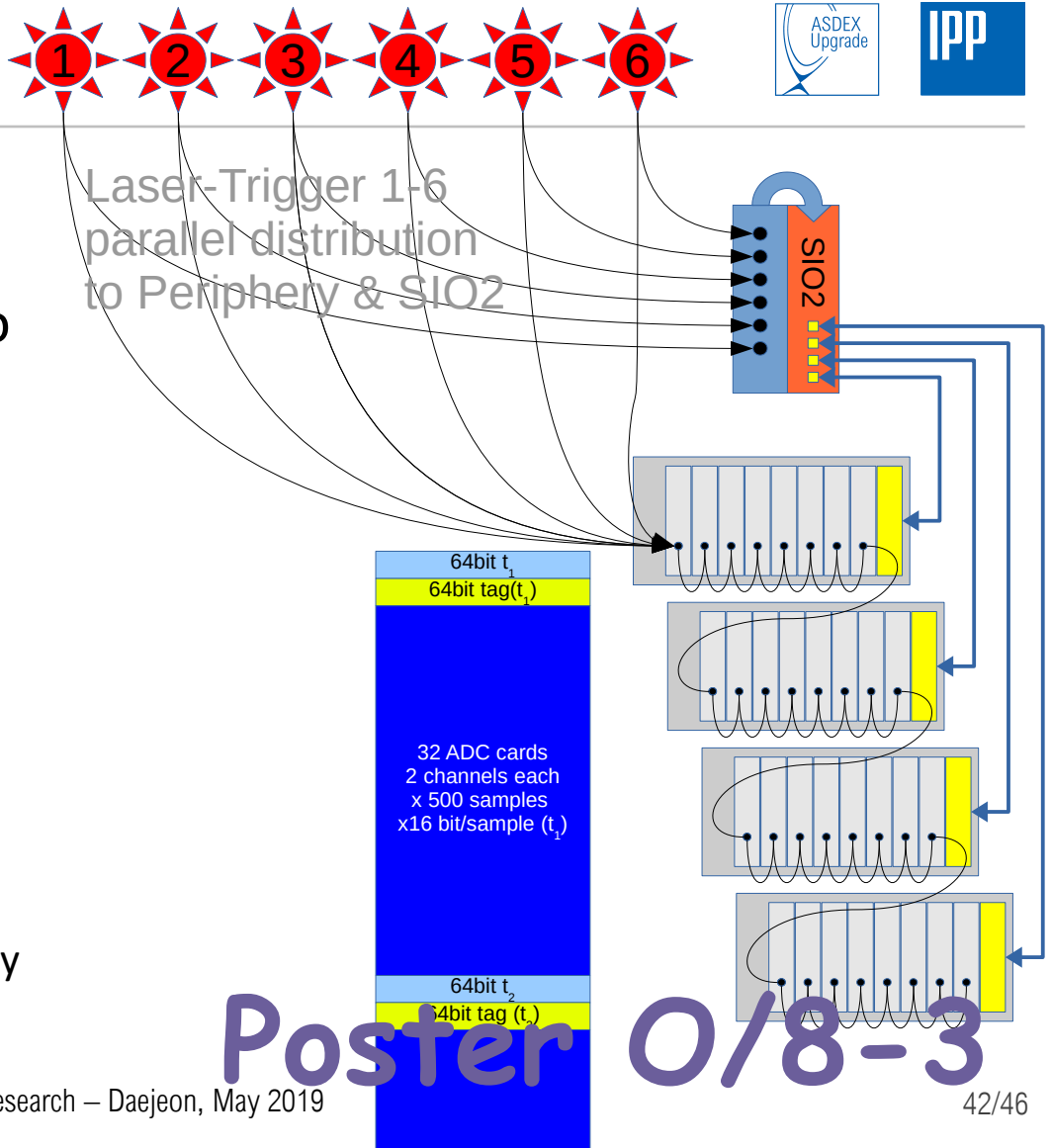



Poster O/8-3

# Six Lasers Interlaced

The planned VerticalTS redesign

- To distinguish between lasers an additional „tag“ is integrated into each SIO data frame
  - The tag is generated by the external trigger logic implemented as FPGA extension
  - Timestamps and tags are stored in FIFOs while the ADC modules sample the time wondows for each laser
  - SIO2 FPGA merge engine combines a timestamp, a tag and the corresponding samples from the periphery in a deterministic way to aggregate data frames for each scattering event
  - Frames are transferred to the host as they arrive in the SIO2 DMA up-stream FIFO




Poster O/8-3

# Summary

- The Pipeline Backplane with its FPGA controller card is a concept to aggregate „simple“ easy to build input channels into a fast deterministic low latency multichannel real-time DAQ environment.
- The SIO2 computer interface card is an FPGA implementation to control the configuration, operation, timing, and data collection from multiple Pipeline crates with multiple signal channels into computer memory in real-time.
- New ADC channels for the Pipeline concept were designed or are under way to support advanced diagnostic requirements:
  - 4-ch. legacy HOTLink receiver card for the refurbishment of Soft-X-Ray and Mirnov diagnostics
  - 20 MHz ADC card for the fluctuation detection Doppler-Reflectometry (not mentioned in this talk)
  - 2-ch. 1 GHz ADC card, 10-bit effective amplitude resolution for Thomson Scattering
- Special SIO2 FPGA upgrades have been developed for Thomson Scattering:
  - triggering of a DAQ cycle by an external event (via a trigger pulse input extension card)
  - queued triggering and read-out of up to six TS bursts (in combination with the 1GHz TS ADCs)

# Thank you and

I‘d like to thank all people involved in this work

the roots dating back more than 30 years

for their

great contributions
fathomless patience
awesome creativity
unprecedented commitment

# Questions?

- Why don‘t we use commercial NI-RIO FPGA cards for DAQ?
  - Yes, it is possible to modify the pipeline controller card so it adapts to the NI-RIO input/output channels. With an appropriate set-up in the NI-RIO FPGA you are able to use the pipeline periphery with an NI-RIO interface.
    However, you will loose the deterministic AUG central experiment time connectivity and the timing features built into the SIO2.
    Nevertheless, this can be partly substituted using an AUG time to digital converter (TDC) within such a system to provide at least the central experiment clock counter and a limited timestamp generation feature to that system.
- What about the future of the SIO2 / Pipeline system?
  - The Pipeline concept is a living development of the ASDEX Upgrade CODAC group. New requirements have to be discussed as they arise and might become implemented if agreed upon.
  - The current SIO2 development comes to an end as a couple of the involved people retire (or have retired). Nevertheless, a transfer of the knowledge behind SIO is intended and future has to show if this concept will still be of interest. Meanwhile, to support the refurbishing of elderly diagnostics with this concept in the near future, a number of SIO2 cards and corresponding Pipeline Controller cards have been built on stock. This might hold for another couple of years ¿3-5?.
  - Concepts for a 3rd generation of SIO cards might feature a couple of modifications (presuming a rejuvenated SIO team):
    - Replacement of the current FPGA by a faster up-to-date device
    - Enhanced 4x, 8x, 16x PCIe Gen4 computer interface (as consequence of a replaced FPGA)
    - New high density super fast optical links (one connector, 6-12 bidirectional optical links)
    - Change card format to low-profile PCIe (fits more easy into modern computers)

# Continuously Clocked DAQ – the default case

SIO was designed for this type of DAQ and most diagnostics are like that.

- Clock ticks from the SIO FPGA pacing all periphery channels in lockstep
- A very simple timing program:
  - Start sampling at a certain central clock count sent via network from Plasma Control
  - Do a timestamp and a periphery data collection cycle for each trigger tick
  - Build a „frame“ and send to host memory
- This operation mode works up to sampling frequencys of 2 MHz
- Up to 256 ADC channels have been aggregated in one host computer
- The amount of data acquired during one plasma discharge is limited only by the amount of reserved host computer memory
- Sustained bandwidth achied for diagnostics
  - Soft-X-Ray: 1 GiB/s (256 MiB/s per SIO2 card)
  - Mirnov Probes: 512 MiB/s (256 MiB/s per SIO2 card)
  - Divertor X-UV bolometer diodes: 64 MiB/s