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Implementation of an FPGA-based DAQ and Processing system for Neutron-Diagnostics using Nominal Device Support, OpenCL and MTCA

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Thanks to their flexibility, FPGA-based Data Acquisition (DAQ) and processing systems are well suited to develop applications that are standard, modular, maintainable and scalable. There is currently a variety of FPGA-based solutions implementing DAQ systems and there are different approaches to design the hardware inside the FPGA. Each approach has its advantages and drawbacks, in terms of ease of the design cycle, performance, and portability among technologies. The solutions chosen by ITER CODAC use traditional HDL-based tools for MTCA-based systems or LabVIEW/FPGA and IRIO open source tools for PXIe systems (FlexRIO) and cRIO. The purpose of IRIO is to simplify the development cycle and the integration with EPICS. The main drawback is that LabVIEW/FPGA is only valid for hardware targets developed by one manufacturer. In this work, we evaluate a new approach valid for DAQ devices of multiple hardware architectures and manufacturers. This approach relies on the use of a new framework, which combines the power of software driver standardization provided by ITER with Nominal Device Support (NDS v3) with the portability and short development cycle provided by hardware description using OpenCL standard for FPGAs. NDS creates an abstraction layer, which separates the control system interface from the device driver implementation. The hardware description is done in OpenCL by means of Kernels that are managed by the host using the OpenCL runtime library. With these tools combined, the device driver is independent of the control system, while also being compatible with any hardware supporting OpenCL. Besides, we gain the heterogeneous processing capabilities of OpenCL.
In this work, the advantages of this approach, called IRIO-OpenCL, will be demonstrated. A use case for data acquisition and processing system is implemented to estimate the fusion power through the average neutron flux emitted by the plasma. Measurements for this use case originate from detectors on a fission chamber. The DAQ system digitizes the pulses produced by the neutrons in the fission chamber and, applies hardware signal processing algorithms such as filtering to increase the signal to noise ratio, or the three most used algorithms to estimate the neutron flux: Pulse Counting, Campbelling, and Current counting. All the high-performance tasks of acquiring and processing involved in the algorithms are carried out by hardware executing the OpenCL kernels.
On the hardware side, the system uses a MTCA chassis with a carrier hub, which provides an optical PCIe interface, connected to the host computer. The acquisition and processing device is the N.A.T Advanced Mezzanine Card (AMC) module NAMC-Arria10-FMC board. This board consists of an IntelFPGA ARRIA10 and includes a FMC (FPGA Mezzanine Card) connector where the AD-DAQ2FMC-EBZ module providing two 1GS/s ADC channels together with two 1GS/s DAC channels is installed.

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