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Methodology to standardize the development of FPGA-based intelligent DAQ and processing systems on heterogeneous platforms using OpenCL

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The usage of FPGA-based DAQ systems has been growing in instrumentation and control systems for Big Science experiments over the last years. The combination of flexibility and performance that FPGAs give to DAQ and processing systems for diagnostics is unrivaled. Moreover, the tasks for which FPGAs are used have been increasing in number and complexity, for instance, data acquisition, processing algorithms, complex timing and triggers mechanisms, interlock operations, or machine-learning algorithms. The ITER hardware catalog for fast-controllers defined by CODAC includes FPGA-based PCIe devices for PXIe and MTCA platforms. Nevertheless, design cycles for FPGA based applications are still complex and costly. At present, three options exist to develop for FPGAs: hardware description languages (VHDL, Verilog/SystemVerilog), graphics languages like LabVIEW/FPGA; and high-level languages such as HLS languages or OpenCL. From these, HDLs are the most complex to use, but they offer the highest flexibility and control over the implementation, while not being bound to a particular hardware manufacturer. Alternatively, LabVIEW/FPGA is easier to use, but it is constrained to specific hardware (ITER uses LabVIEW to develop for FlexRIO and cRIO devices). Lastly, HLS languages and OpenCL enormously simplify the hardware description using high-level languages like C/C++ which are also hardware agnostic. Additionally, standardization adds value to high-level languages, reducing the development times, to the extent that modules or complete software layers can be reused.
The work presented here is a set of methods and tools that allow developing applications for FPGA-based instruments in a standardized way, using the following elements: an OpenCL compliant Board Support Package for a PCIe device; an OpenCL interface to communicate with high-speed AD/DA converters using the JESD204B standard; a set of OpenCL Kernels to support common DAQ functionality, capable of acquiring and processing at high sampling rates; and a standardized software interface, including the NDS software layer supported by ITER that integrates the whole solution with EPICS.
The methodology has been validated with the implementation of an estimator of the fusion power through the average neutron flux on a MTCA FPGA-based DAQ and processing platform. A discussion is provided on how this methodology simplifies integration and improves maintainability compared to other development languages and tools.

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