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Evaluation of the Backup Signal-Processing System of the KSTAR Quench Detection System

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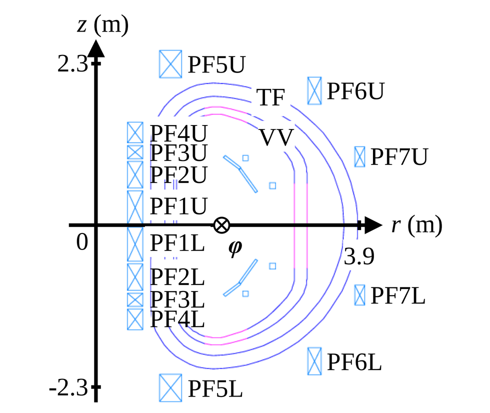
1. Abstract

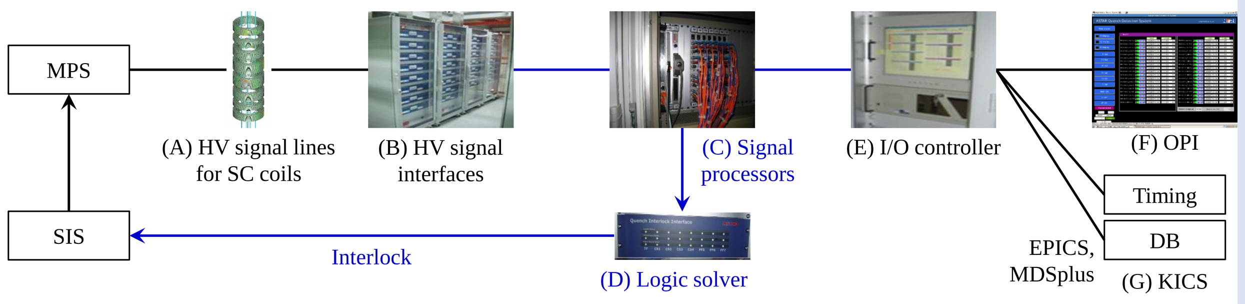
- The KSTAR Quench Detection System (QDS) has been operated to protect the superconducting coil system of the KSTAR device for 11 years.
- A backup signal-processing system of the QDS is being developed mostly using Commercial-Off-The-Shelf (COTS) devices. Both the VME systems and the backup system simultaneously operate to detect quench, which alarms are voted by 1-out-of-2 (1oo2) logic to generate interlock signals, in normal operation.
- The backup system was integrated with the QDS, and its components for the Poloidal Field 1 (PF1)–PF4 coils were tested in the KSTAR campaign 2018.

2. Quench Detection System

- Quench is a phenomenon of unrecoverable thermal runaway in superconductors by breaking critical conditions: temperature, magnetic field, or electrical current density. The superconductors have to be immediately discharged to prevent from overheating themselves in the event of quench. Quench may be detected by discriminating a change of physical parameters such as conductor voltage or coolant temperature.
- The QDS mainly consists of High Voltage (HV) signal interfaces with 83 channels of voltage taps, 3 sets of VME systems with a host computer, and 1 set of a logic solver. The QDS discriminates a normal voltage of ~100 mV on NbTi or Nb_3Sn Cable-in-Conduit Conductors (CICCs) in the event of quench, while the PF coils are applied with voltages of up to some kV by pulsed operation of the Magnet Power supply System (MPS). Induced voltages on the coils are compensated by quench detection circuits in the HV signal interfaces and digital signal processors of the aged VME systems.
- An allowable delay time to detect quench is about 3 s. Discharge time constants are 4 s, 7 s, and 360 s in the cases of PF, Toroidal Field (TF) fast, and TF slow discharges, respectively. A Mean Time Between Failures (MTBF) of the QDS has to be better than ~4 months according as the lengths of annual KSTAR operation periods.



Arrangement of the KSTAR Coils



KSTAR Quench Detection System

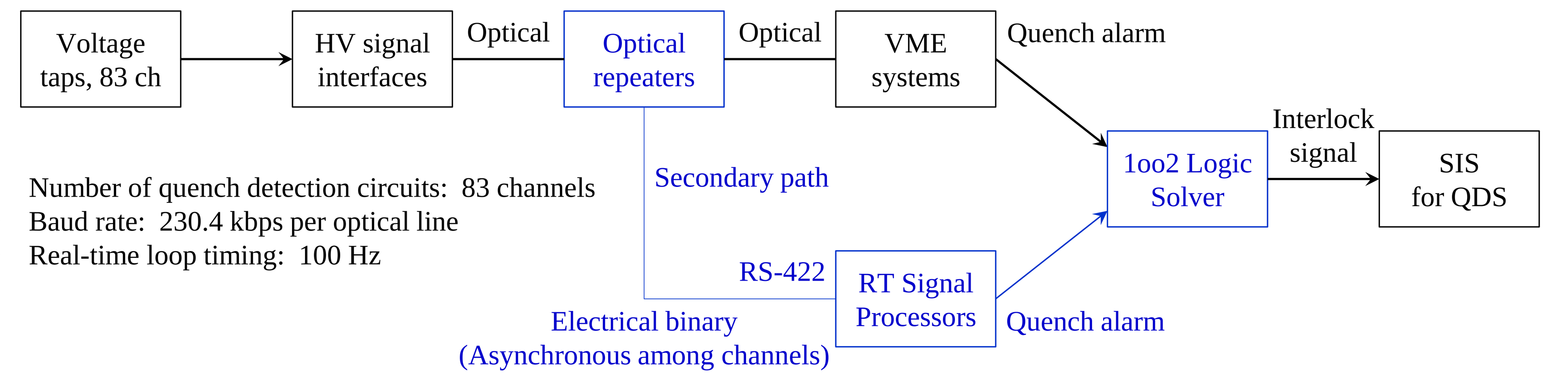
Quench Detection Criterion
Threshold: ~100 mV
Holding Time: 1–3 s

$$V_k = \left(M_{kk}\dot{I}_k + R_k I_k\right) + M_{kj}\dot{I}_j + M_{pk}\left(\dot{I}_p + Z\dot{I}_p + R\dot{I}_p + \cdots\right) \quad \text{for } k, j = \text{coil numbers}$$

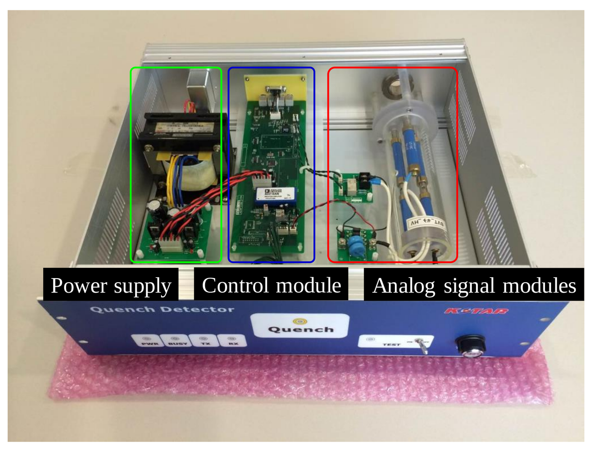
(1) Self-driven voltage by k-th element
(2) Mutually driven voltage from the other coils
(3) Induced voltage driven by various plasma dynamics

3. Concept of the Backup Signal-Processing System

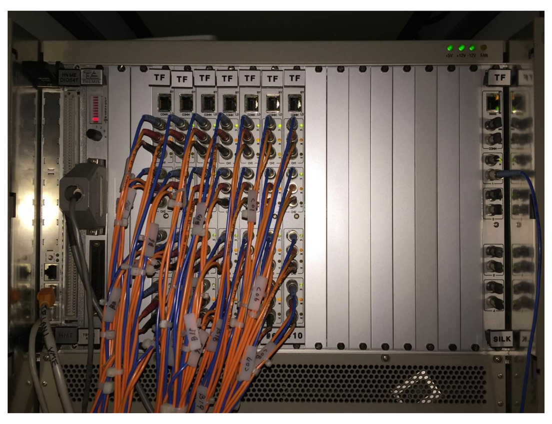
The backup signal-processing system duplicates the path of quench detection signals while the existing components operate with no change. The backup system conducts quench detection by using hardware logics including FPGAs; whereas, the VME systems are using CPUs for quench detection. Both the VME systems and the backup system simultaneously operate to detect quench, which alarms are voted by 1oo2 logic to generate interlock signals, in normal operation. The backup system may take over the total functions of the VME systems if the VME systems break down.



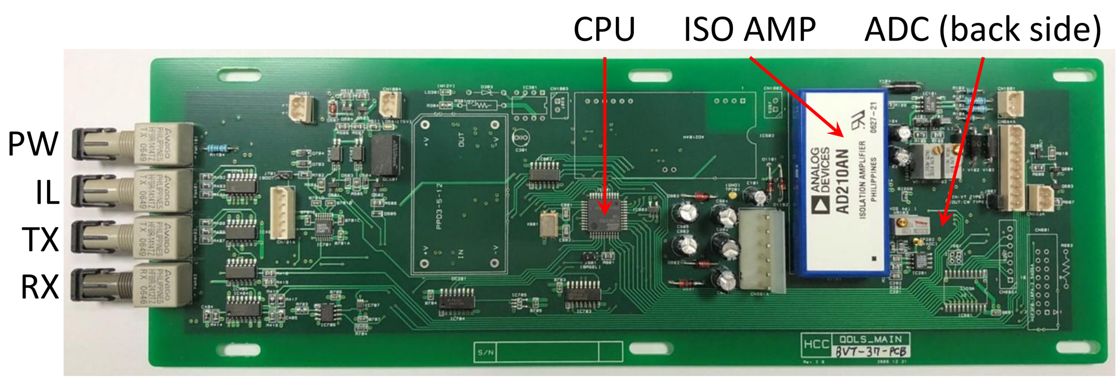
Schematic Signal Flow of the QDS with a Backup Signal-Processing System



HV Signal Interface, 83 sets



VME System, 3 sets



Parameter	Description
Input Signal Range	±1 V
Input Signal Isolation	AD AD210AN, 2.5 kV rms
Low-Path Filter	Sallen-Key 4th, 4 Hz
A/D Converter	AD AD7894, 14 bit
Sampling Rate	100 Hz
Sample Clock	Internal, asynchronous
CPU	Atmel AT89C51ID2, 8 bit
Data I/O	UART, Optical, 230.4 kbps

Control Module of the HV Signal Interface, 83 EA

4. Results of the Development and Operation

The optical-signal repeater performs (1) Pass-through of the optical signals between the HV signal interface and the VME system, (2) Wiretapping of the optical signals for the RT signal processors, and (3) Switch of the supervisory system: the VME system or the backup system. All the functions were operational.

Optical-Signal Repeater, 3 sets

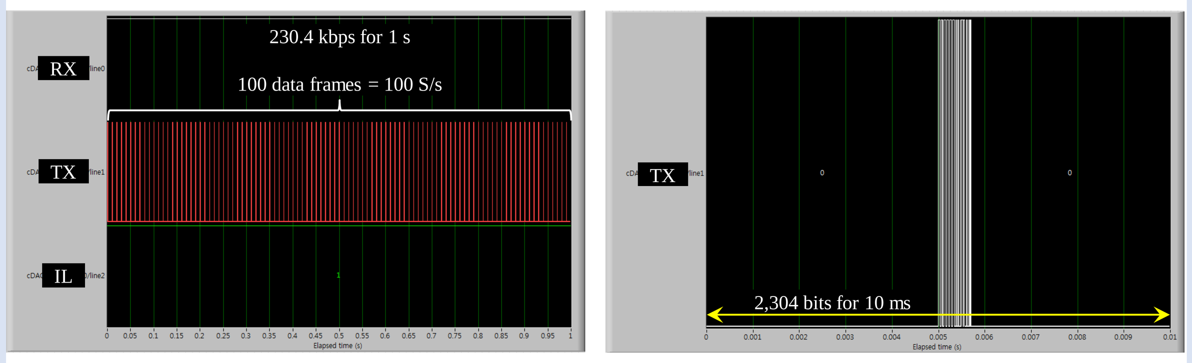
Parameter	Description
Platform	VME rear transition-wise module, 6U, 2 ch / module (No control/data through a backplane)
Bit Frame	UART, 230.4 kbps baud rate, 8 data bits, 1 stop bit, no parity
Optical I/O	820 nm wavelength, TX: Avago HFBR-1414TZ ; RX: Avago HFBR-2412TZ
Electrical I/O	RS-422

Data Frame from the HV Signal Interface to the VME System

1	2	3	4	5	6	7	8	9	10	11	12
Header	Status	ADC Raw		Quench Duration Time		Threshold value		Check time		CRC	CRC
0x80	0x08	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	-	-

Command Frame from the VME System to the HV Signal Interface

1	2	3	4	5	6	7	8	9
$	S	1	HH	HL	LH	LL	CR	LF
0x24	0x53	0x31	MSB		LSB		0x0d	0x0a



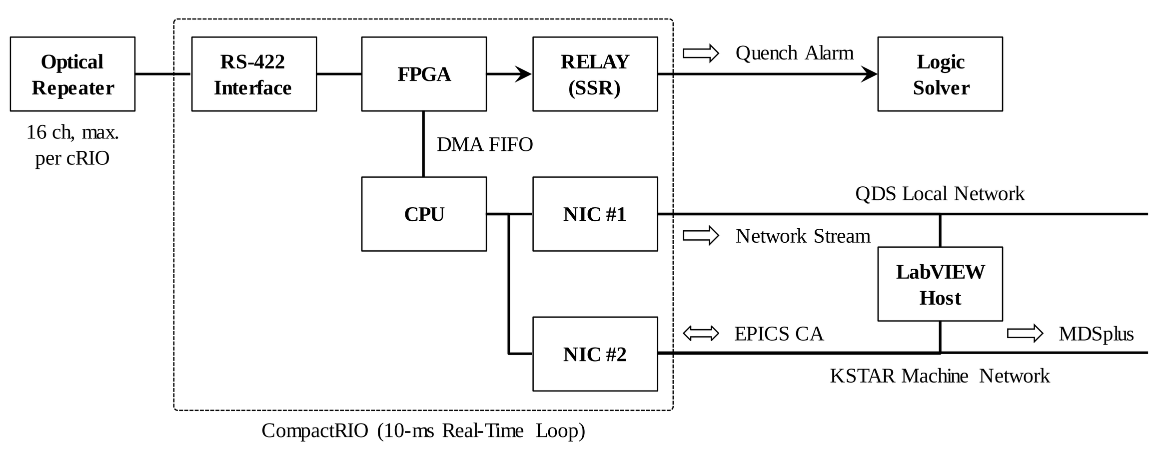
Wiretapped Signal on an Optical TX Line from the HV Signal Interface

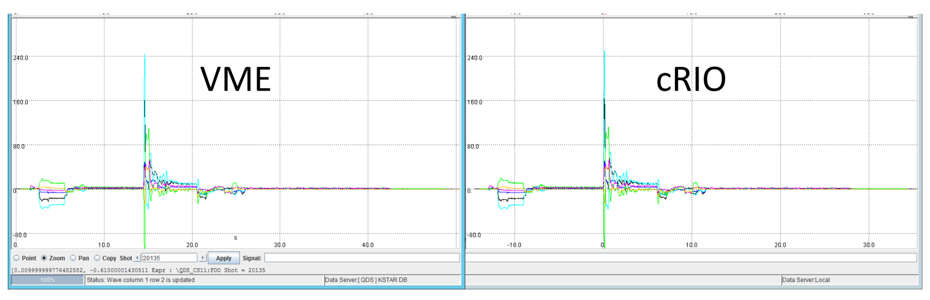
The real-time signal processor performs (1) Numerical compensation of induced voltage on the quench detection circuits, and (2) Decision of quench. All the functions were operational.

- FPGA: Data I/O, quench detection signal analysis, and relay output.
- CPU: EPICS server, network stream server.

CompactRIO System (Right One), 7 sets

Item	Existing System (3 VMEs)	Backup System (7 cRIOs)
Platform	VME64, WxWorks	NI CompactRIO, LabVIEW RT
Controller	TF SBC: Motorola MVME5110 - MPC7410, 400 MHz, 256 MB RAM PF SBC: GE VG5-V3.3 - MPC7457, 867 MHz, 256 MB RAM	NI cRIO-9039 (*) - Intel Atom E3845, 1.9 GHz, 2 GB RAM - Xilinx Kintex-7 7K325T, 16 ch DMA (*) Also using NI cRIO-9049
Data I/O (TX, RX)	Optical I/O (HMT QDIS2 LINK) - UART at 230.4 kbps per line	Optical Repeater (UWS QDS OR1), RS-422 modules (NI 9871) - 230.4 kbps per port
Quench Alarm	Optical Output (HMT QDIS2 SILK), Optical / Relay Converters - Normally High	Relay (NI 9485) - Normally Closed



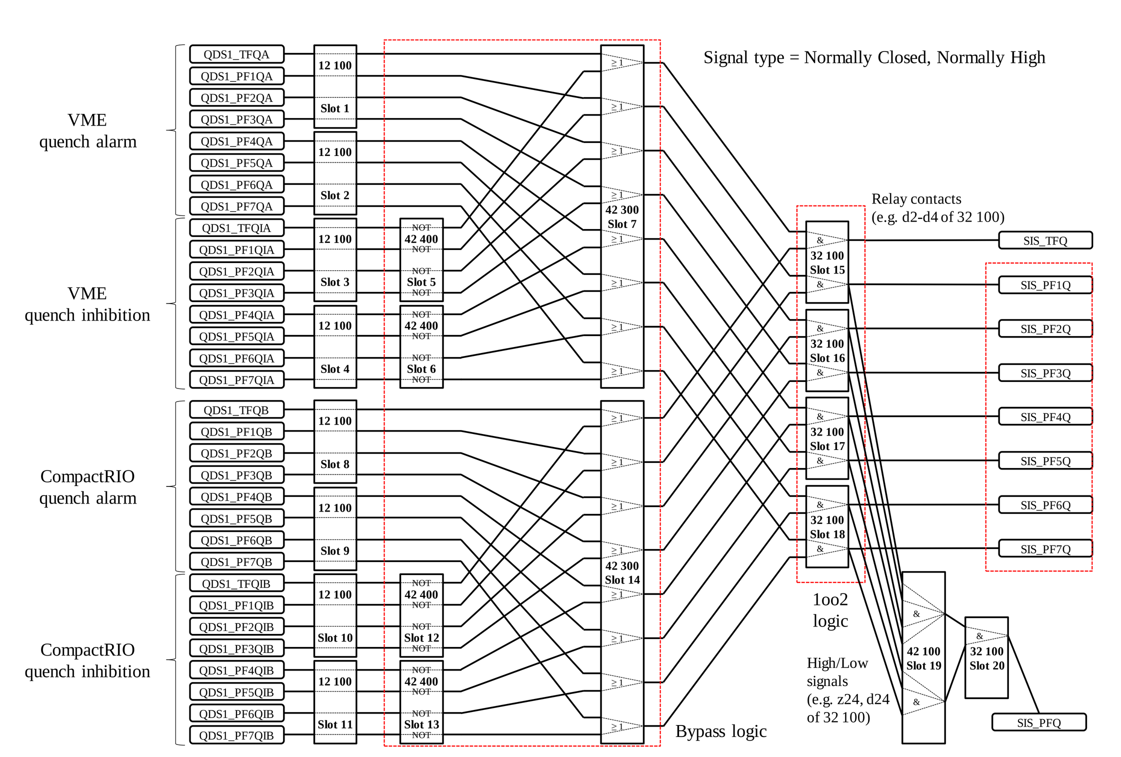


Quench Detection Voltage Acquired through the VME and CompactRIOs

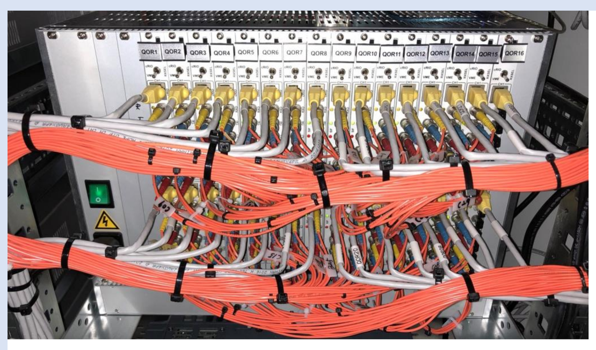
The logic solver performs (1) Logical operation with the quench alarms and the inhibit signals, and (2) Decision of interlock. All the functions were operational.
HIMA Planar4 is a safety controller configured by hard-wiring, which may achieve at Safety Integrity Level 4 (SIL 4).

HIMA Planar4, 1 set

Slot	Module	Part number	Description
1	4 channel input module, SIL 4	12 100	Inputs from VME: Quench alarm TFQA - PF3QDA
2	4 channel input module, SIL 4	12 100	Inputs from VME: Quench alarm PF4QA - PF7QDA
3	4 channel input module, SIL 4	12 100	Inputs from VME: Quench inhibition TFQA - PF3QDA
4	4 channel input module, SIL 4	12 100	Inputs from VME: Quench inhibition PF4QA - PF7QDA
5	4-fold blocking element	42 400	NOT of quench inhibition TFQA - PF3QDA
6	4-fold blocking element	42 400	NOT of quench inhibition PF4QA - PF7QDA
7	8-fold OR element with two inputs each	42 300	OR of alarm and inhibition
8	4 channel input module, SIL 4	12 100	Inputs from cRIO: Quench alarm TFQB - PF3QDB
9	4 channel input module, SIL 4	12 100	Inputs from cRIO: Quench alarm PF4QB - PF7QDB
10	4 channel input module, SIL 4	12 100	Inputs from cRIO: Quench inhibition TFQB - PF3QDB
11	4 channel input module, SIL 4	12 100	Inputs from cRIO: Quench inhibition PF4QB - PF7QDB
12	4-fold blocking element	42 400	NOT of quench inhibition TFQB - PF3QDB
13	4-fold blocking element	42 400	NOT of quench inhibition PF4QB - PF7QDB
14	8-fold OR element with two inputs each	42 300	OR of alarm and inhibition
15	2 channel relay amplifier, SIL 4	32 100	Outputs to SIS: Interlock TFQ - PF1Q
16	2 channel relay amplifier, SIL 4	32 100	Outputs to SIS: Interlock PF2Q - PF3Q
17	2 channel relay amplifier, SIL 4	32 100	Outputs to SIS: Interlock PF4Q - PF5Q
18	2 channel relay amplifier, SIL 4	32 100	Outputs to SIS: Interlock PF6Q - PF7Q
19	4-fold AND element with five inputs each	42 100	Inputs from relays: Interlock status TFQ - PF7Q
20	2 channel relay amplifier, SIL 4	32 100	Outputs to SIS: Interlock TFQ and PFQ
21	Communication module, Modbus, RS-485	80 105	Outputs to IOC: Logic solver status



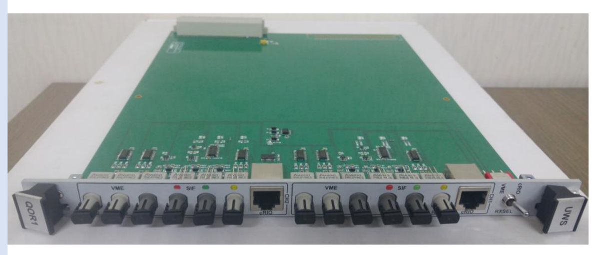
Hard-Wired Logic to Generate Interlock Signals



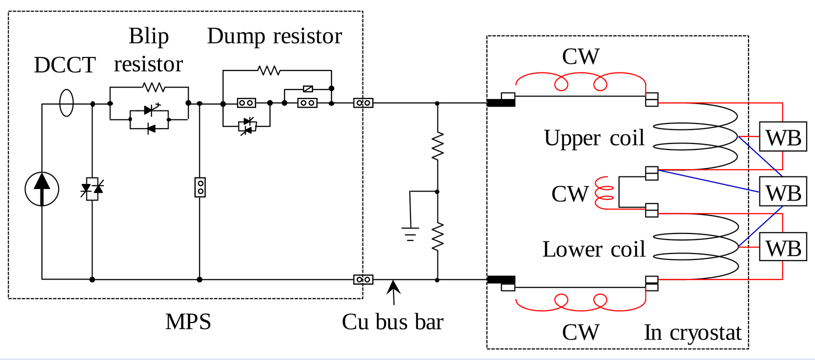
Optical-Signal Repeater, 3 sets

RT Signal Processor, 7 sets

Logic Solver, 1 set



Rear Transition-wise Module, 44 EA



Configuration of Quench Detectors
WB: Bridge Type
CW: Co-wound Type

5. Conclusion

- The backup signal-processing system was integrated with the QDS, and its components demonstrated expected functions for the PF1–PF4 coils in the KSTAR campaign 2018, while the existing components were also fully operational with no modification. The concept of this backup signal-processing system, therefore, seemed acceptable. The total components of the backup system will be tested in the upcoming KSTAR campaign 2019.
- The FPGAs of this backup signal-processing system operated at a RT cycle latency of 10 ms in a time accuracy better than 1 μs, and there was no malfunction during the plasma experiments in the last KSTAR campaign. These FPGAs are planned to be inter-connected by a dedicated RT control network, such as Controller Area Network (CAN) bus, to implement advanced compensation methods of induced voltage on the coils.

Acknowledgement

- The Korean Ministry of Science and ICT supported this work.