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# Design and Development of a Cost Optimized Timing System for Steady state Superconducting Tokamak (SST-1)

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SST-1 timing system is a real time event based trigger generation and distribution system used for the synchronized operation of its various heterogeneous and distributed sub-systems during the plasma discharges. The VME based platform dependent old timing system is exhausted with spares inventory during long period of its existence and also had interface issues with the hardware advancement at subsystems end. The timing system physically consists of two types of modules i.e. central module and sub-system module. The timing and trigger distribution from central module to sub-systems are carried out by a star topology based optical fiber network. A platform independent, stand alone, 1U rack mountable timing system is designed, developed and tested based on Xilinx's Artix-7 FPGAs for real time event (trigger) distribution amongst different subsystems of SST-1. The new system design's objectives being, to adopt same star topology as the old timing system, to support existing optical fiber network, to provide single interface to the heterogeneous sub systems and to have performance parameters, comparable to the old timing system with the minimal modifications on hardware as well as on software part at sub systems end.

As stated earlier, in this new system, single central timing system module can support an interface of maximum of eight (8) subsystem modules in star configuration over optical fiber network. The central timing system module can generate pre-defined experiment event (trigger) sequence in real time with a resolution of 10μs and facilitates event logging at a resolution of 1μs. Each sub-system module can support eight (8) TTL inputs for asynchronous event generation and eight (8) TTL outputs for trigger pulse generation with a resolution of 1μs. Each experiment sequence on central timing module and trigger information on sub system timing modules are configured over Ethernet interface through TCP/IP protocol. Maximum of 255 different events information can flow between sub-system timing system modules through central timing system module. Event latency is observed to be in the range of ~ 4μs over 3m length of optical fiber cable.

Timing system modules are designed using Xilin's Artix-7 FPGA for the programmable resources like RAM, DPRAM using IP cores, implementation of glue-logic timing as well as implementation of serialization-deserialization logic based on asynchronous serial communication protocol for event (trigger) information distribution over fiber optic network. The use of FPGA has helped in minimizing the use of dedicated discrete hardware resources such as memory ICs, high speed serializer, de-serializer ICs and other glue-logic ICs. This platform independent standalone design helped, in avoiding designing and testing of multi-platform cards for VME, PXI systems.

Further development is underway to extend the capability of the timing system, to provide clock synchronization for the sub systems using the same timing system modules and to incorporate GPS based IRIG-B time synchronization interface. This completely new in- house design will be advantageous, as it can be easily be adapted for the time synchronization applications in any small, medium size tokamaks or experimental devices irrespective of their the hardware/ software platforms.

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