Design and Development of a Cost Optimized Timing System for Steady State Superconducting Tokamak (SST-1)

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Institute for Plasma Research

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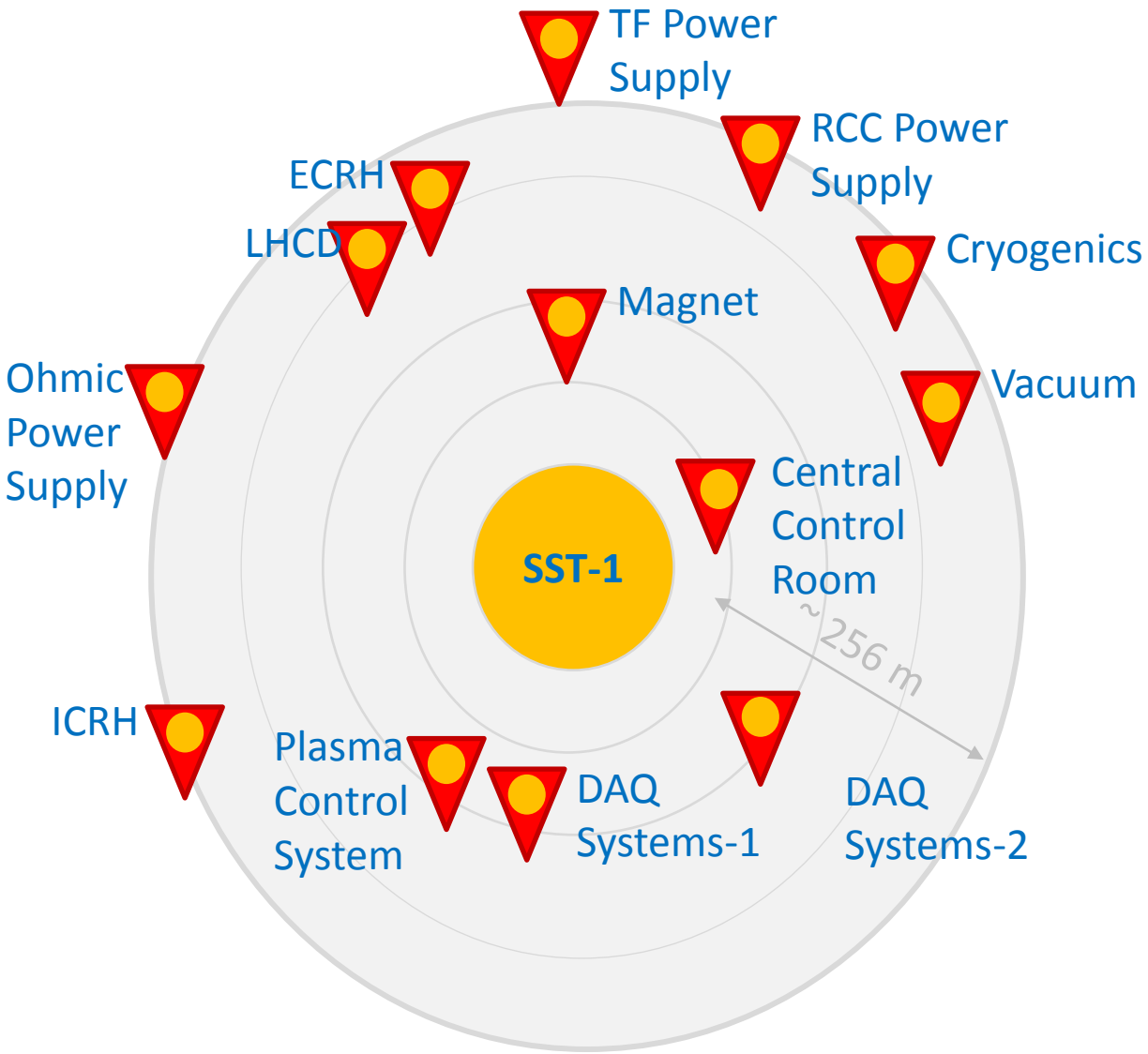
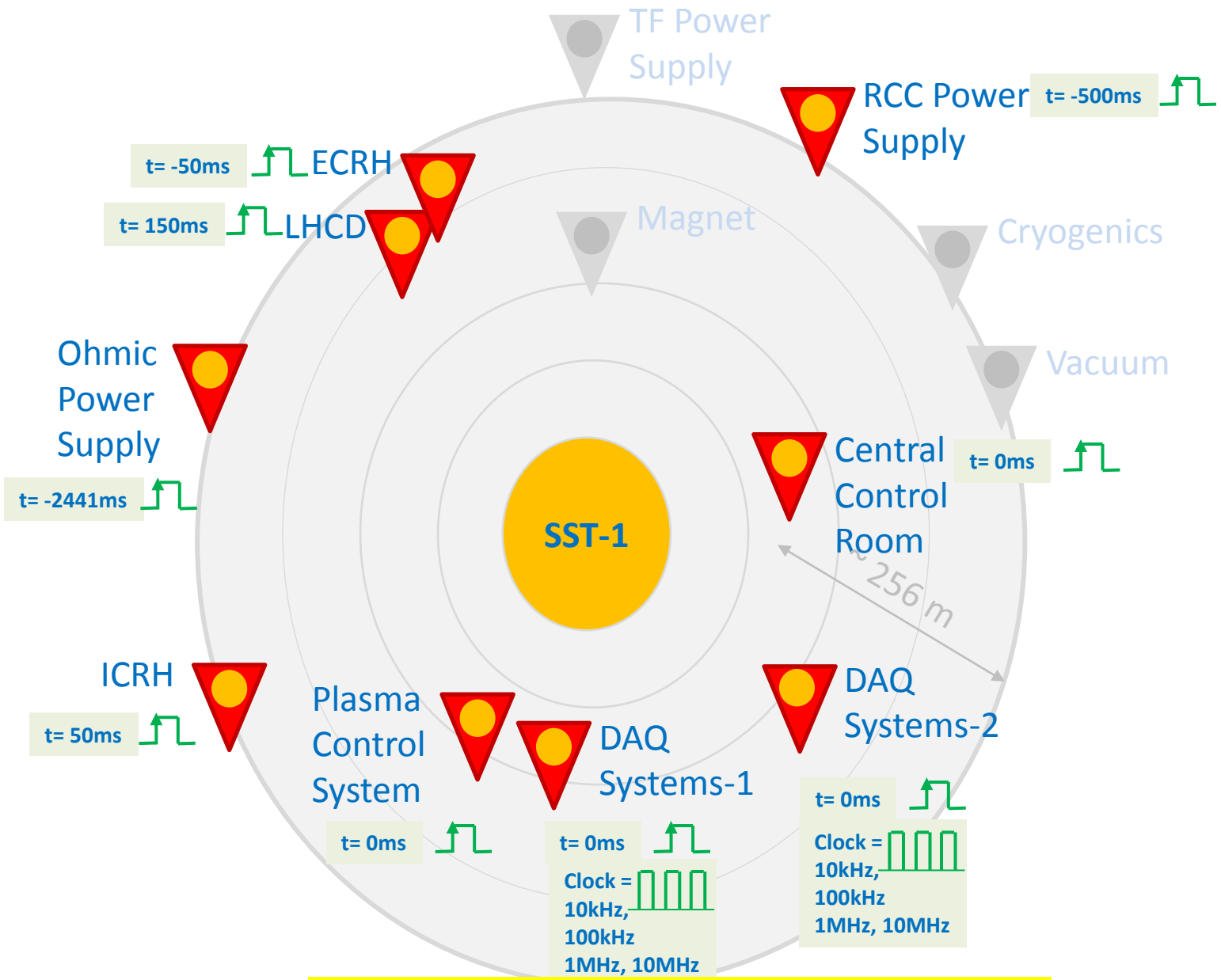
SST-1 sub systems



Spatially distributed & Heterogeneous Platform systems

#Not actual scale (for visualization only)

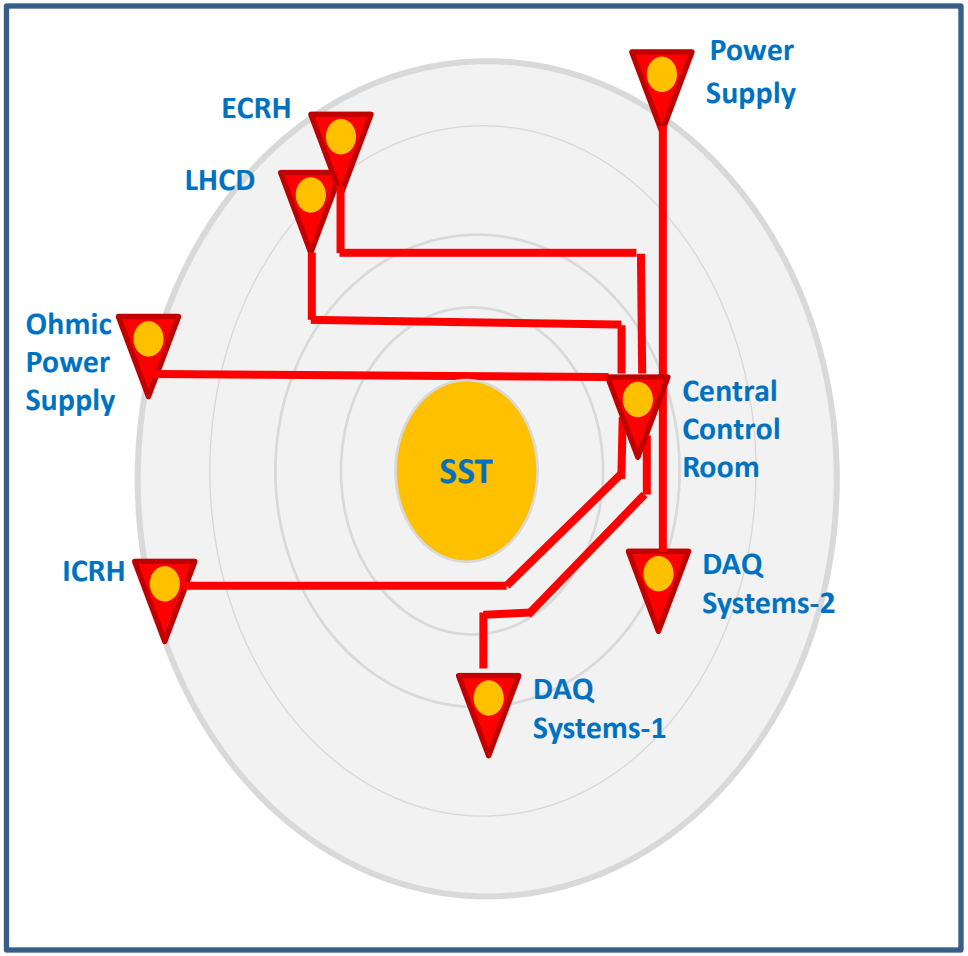
SST-1 sub systems – with Timing System interface



All trigger timings are configurable for all Timing system modules

SST-1 old Timing System

- Based on **VME Platform** (~ 15**Years**). Custom VME Timing System cards were in house designed and developed.
- Master – Slave configuration connected in **star configuration. Optical Network – Multimode, 62.5/125 µm**.
- Provide fast timing signals (**clock & triggers**) to various sub systems during plasma discharges
- Master VME Node (Central Control Room)
  - Broadcast **experiment sequence @ minimum resolution of 1µs**
  - Provide **20MHz Stable OCXO** based clock to slave
  - Record events with **32bit time stamp**
- Slave VME Node (ECRH, Power Supply etc.)
  - Recover & regenerate different clocks (**10MHz,1MHz etc.**) from 20MHz clock
  - Generate different **channel outputs**
  - Provide **optically isolated channel inputs**

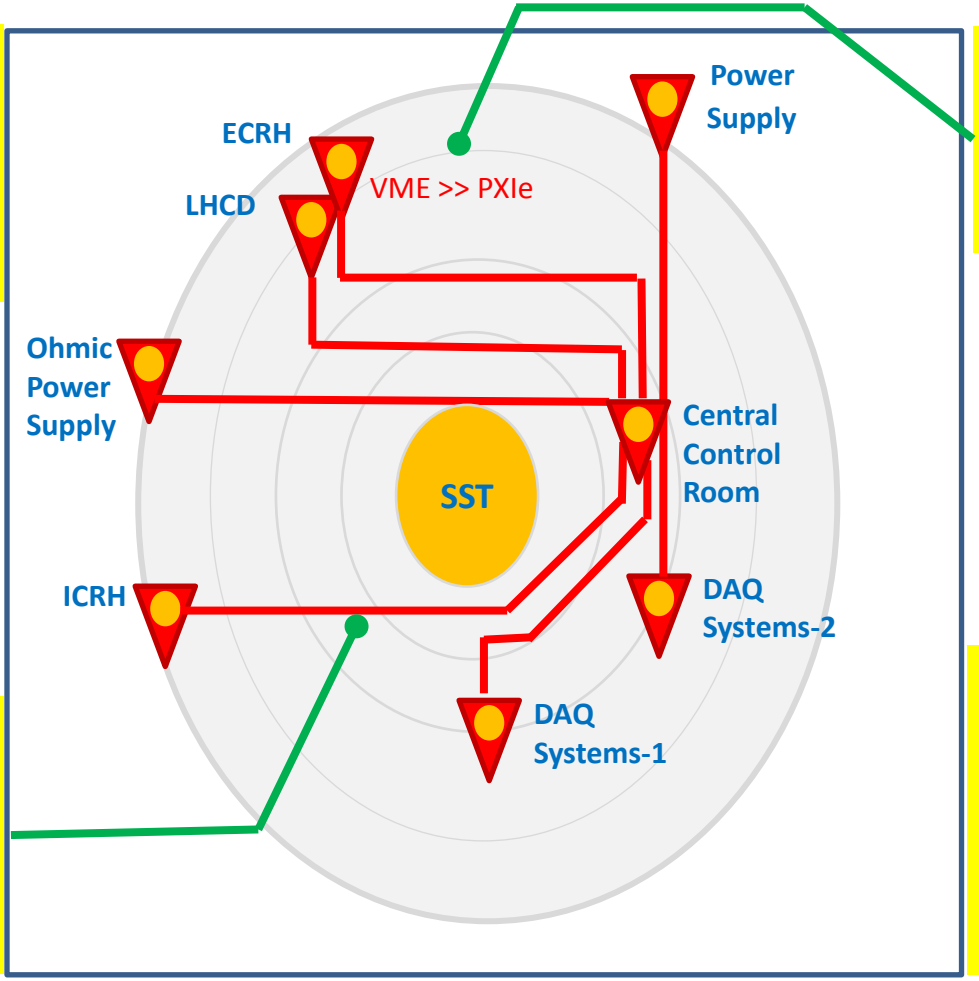


- **Timing System card inventory got exhausted**
- **Sub system hardware advancement also started (Systems migrated from VME to PXI, PXIe etc.)**

Reference:(1)

New Timing System Requirement

1. Timing System with performance parameters comparable to old system

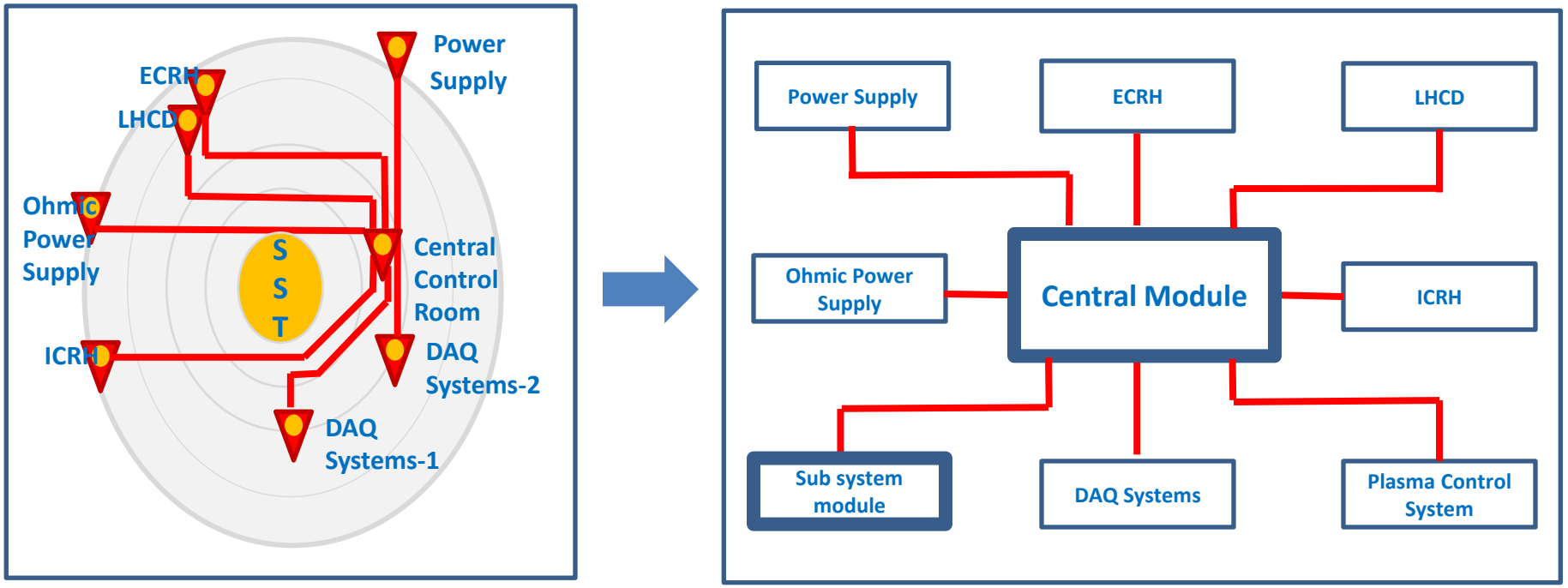


3. Timing System – provide single interface to heterogeneous platform systems

2. Timing System which supports existing optical fiber network and star topology

4. Easy integration with sub system i.e. minimal modification on hardware as well as on software part at sub system end

SST-1 Timing System

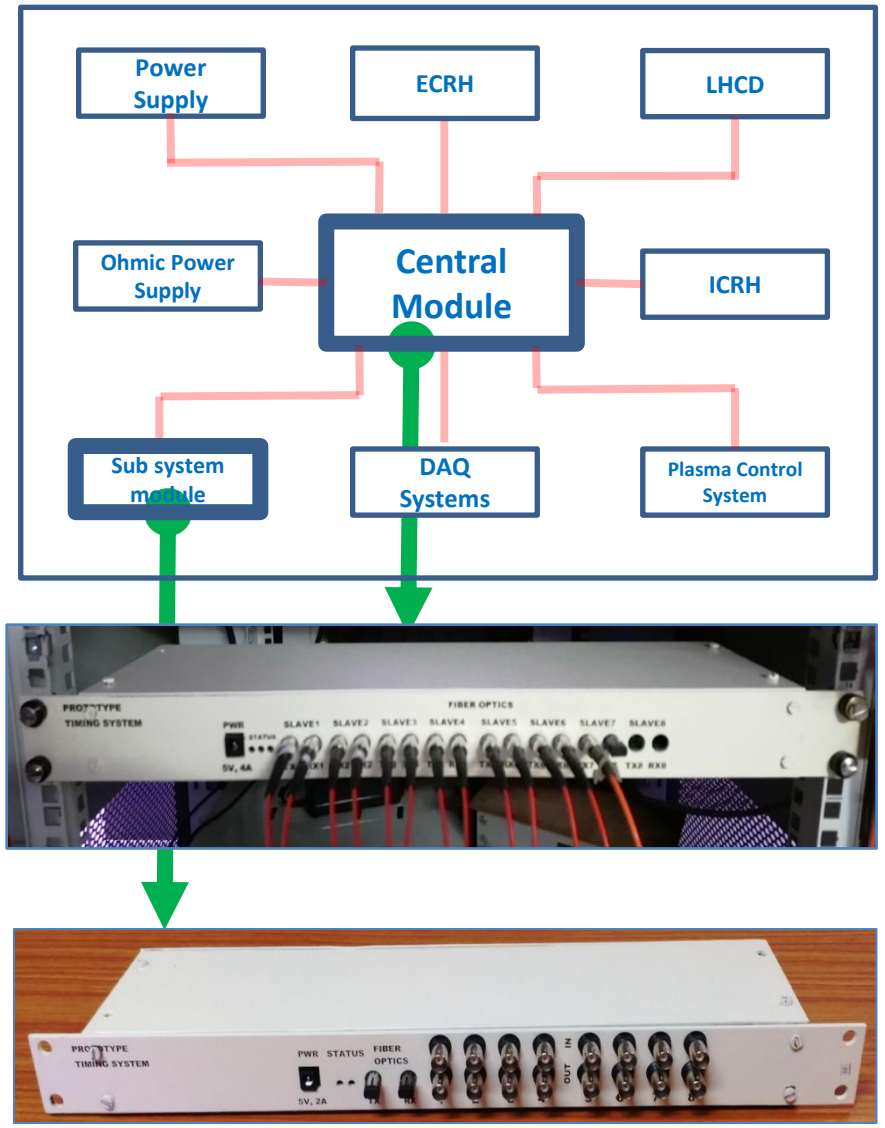


Simplified block diagram- Timing System modules with fiber optic network

Central module(Master), Sub system module (Slave)

SST-1 New Timing System

- **A platform independent**
- **Standalone, 1U Rack mountable modules**
  - Central module (Master)
  - Sub system module (Slave)
- Master – Slave configuration connected in **star configuration. Optical Network – Multimode, 62.5/125 µm**
- Provide **real time event (trigger) distribution** to various sub systems during plasma discharges #
- Modules designed using **Xilinx's Artix-7 FPGA**



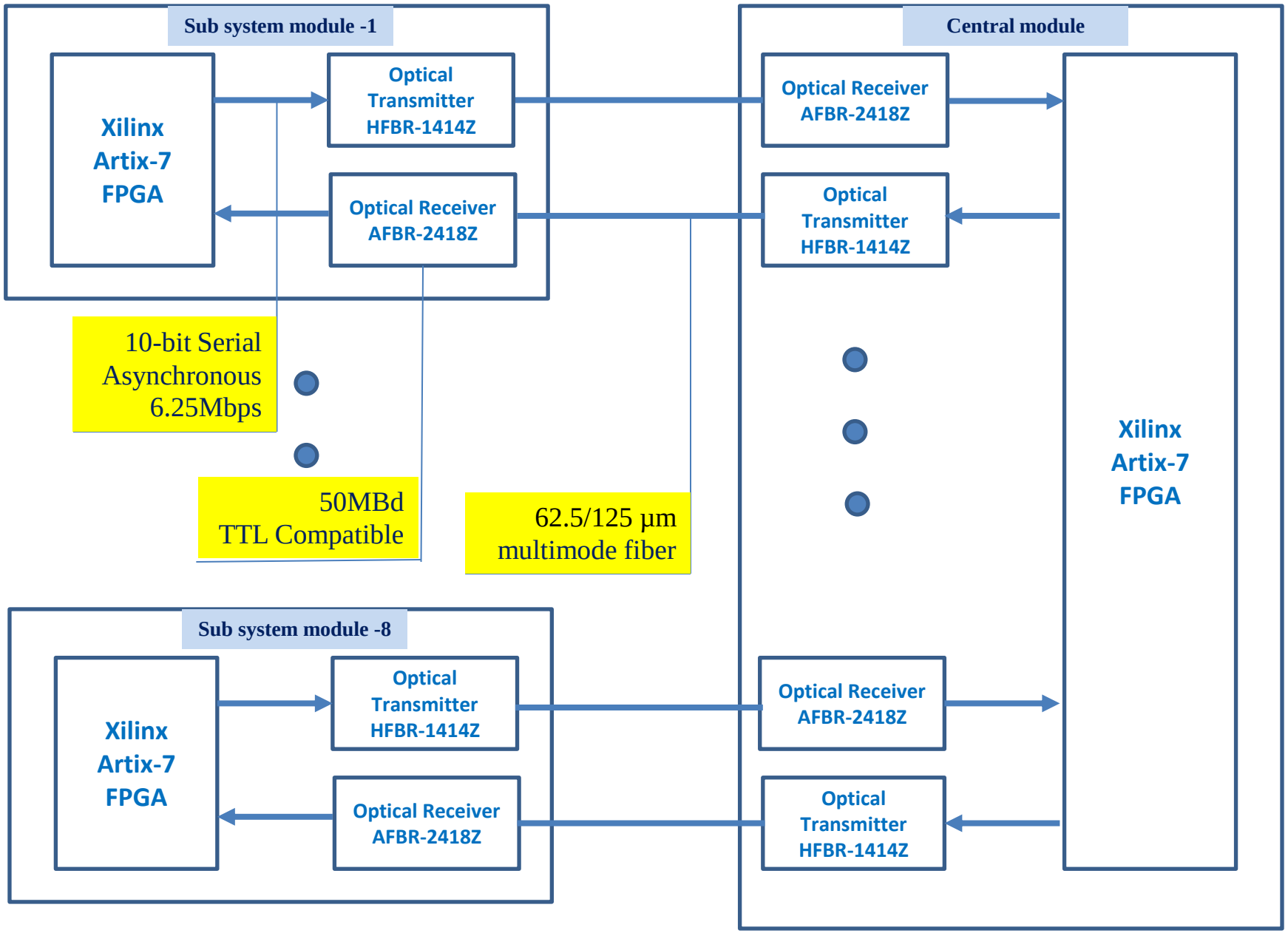
 # Version -1 development boards

SST-1 New Timing System v/s Old

Few Specifications	Old Timing System	New Timing System
Synchronous, Shutdown sequence generation resolution	1 µs	10 µs
Time Stamp resolution of events	50 ns	1 µs
Event latency	3.8 µs (100m optical fiber)	4µs (3m optical fiber)
Real time, Deterministic	Yes	Yes
No. of sub systems that can be connected	16	8
Sub system Asynchronous inputs	16	8
Sub system channel outputs (as triggers)	4 (expandable)	8
Total number of events (reserve events, sync, shut down events …)	65535	255
Trigger output, Asynchronous input signal interface	TTL	TTL
Synchronous Clock distribution	1kHz/10kHz/100kHz/1 MHz/10MHz	Not in present version#
GPS – IRIG B Interface	Yes	Not in present version#

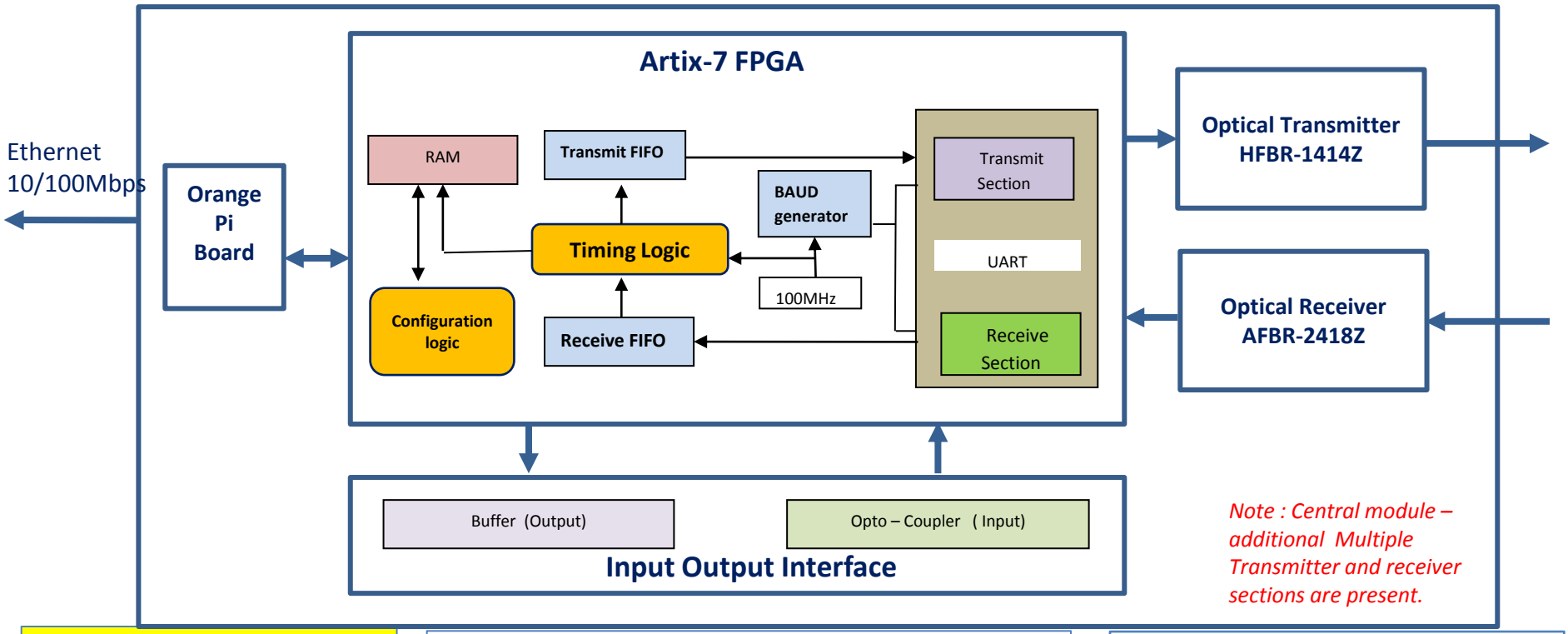
 # Version -1 does not include clock synchronization

Timing System - Central & Sub system modules



Reference:(2,3,4)

Complete Sub System module



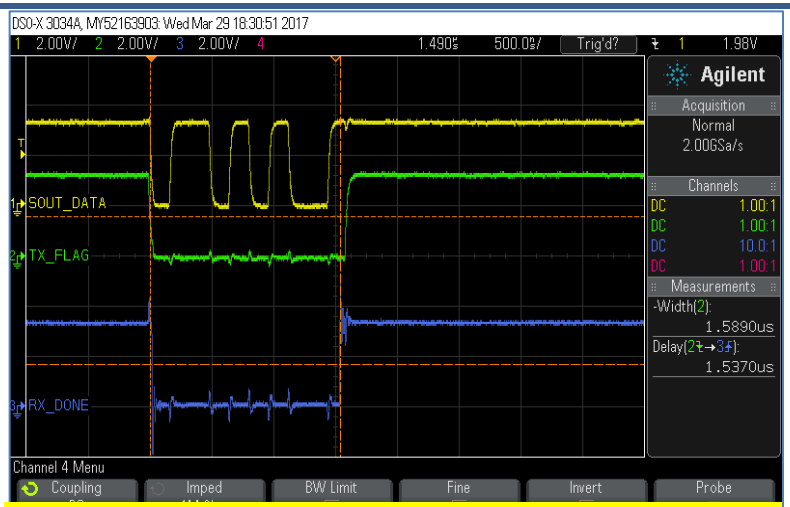
Note : Central module – additional Multiple Transmitter and receiver sections are present.

OrangePi (open-source single-board computer) runs Linux

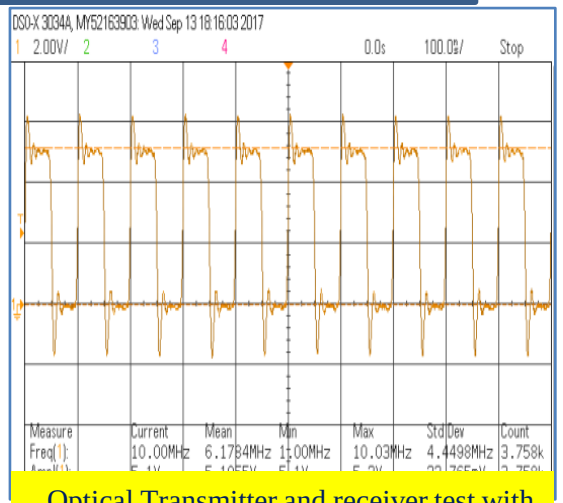
Orange Pi provides Ethernet interface (10/100Mbps) to sub system and central module (for non real time data communication)

OrangePi to FPGA communication – UART 9600bps

Timing System configurations for either sub system module or central module are communicated to FPGA through OrangePi



10 bit data Transmit at 6.25Mbps (8 bit data, 1 start, 1 stop)



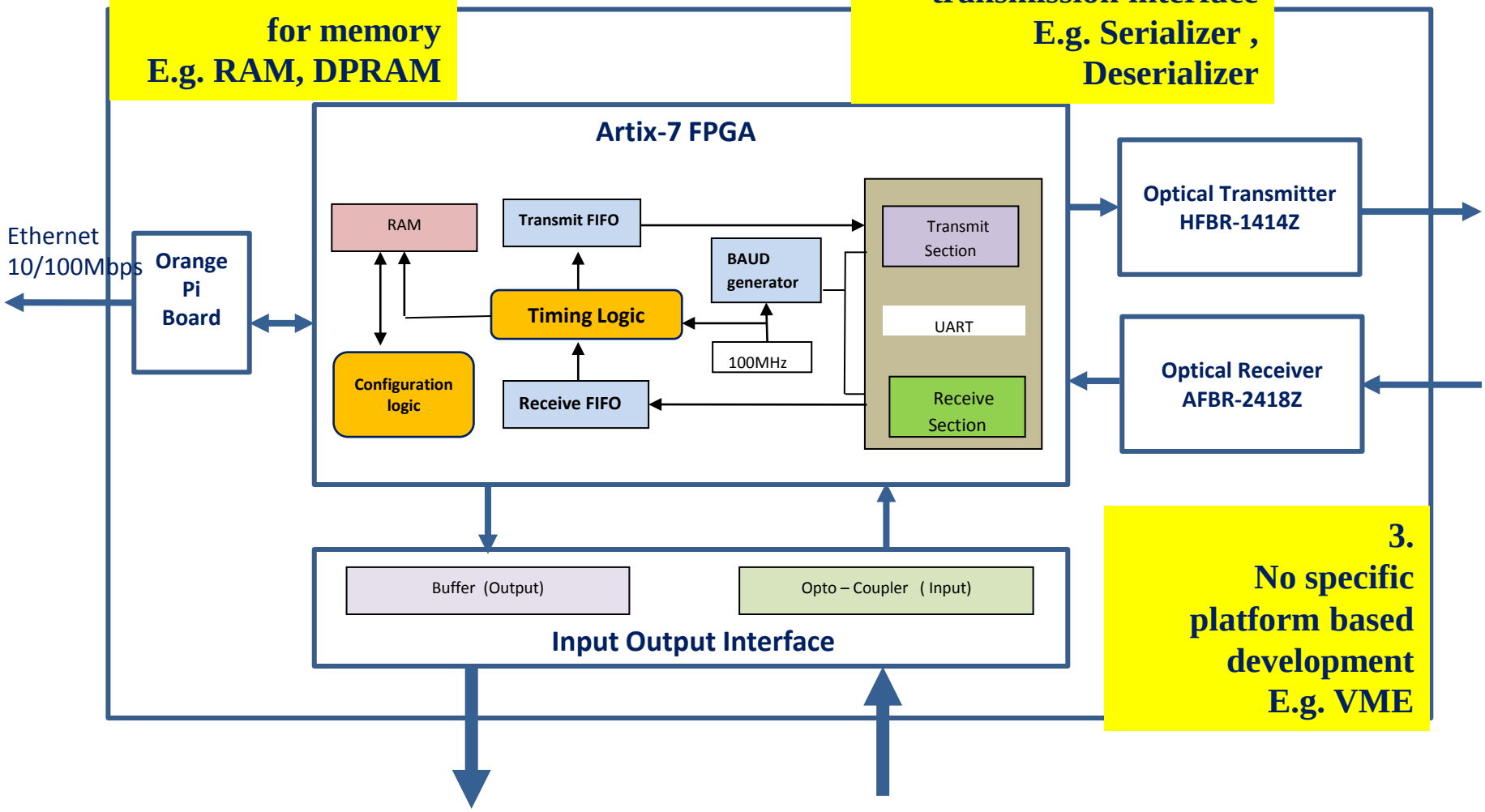
Optical Transmitter and receiver test with 10MHz signal

Reference:(5,6,7,8)

New Timing System – What's difference ?

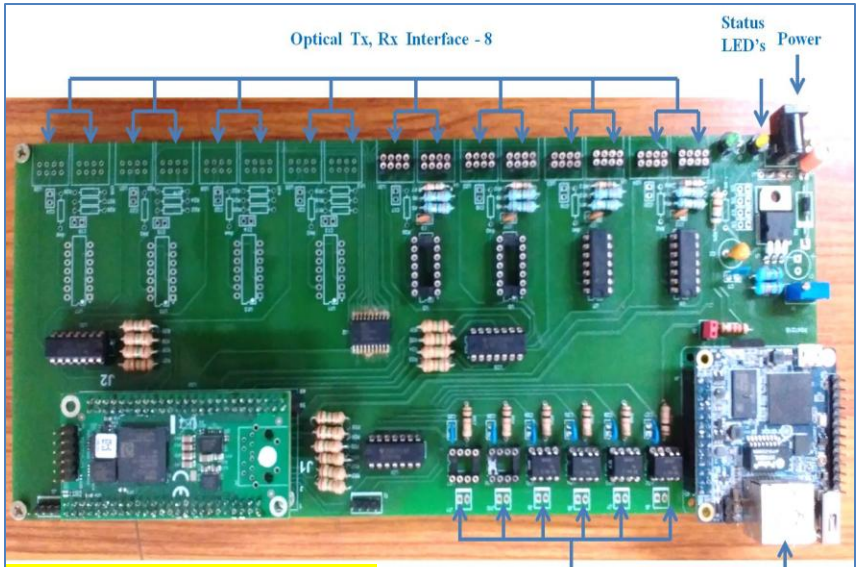
1. No use of dedicated discrete hardware resources for memory E.g. RAM, DPRAM

2. No use of dedicated discrete hardware resources for optical data transmission interface E.g. Serializer , Deserializer



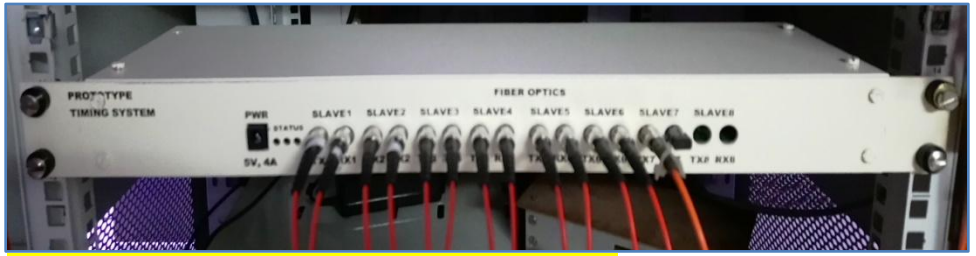
3. No specific platform based development E.g. VME

Central & Sub system modules

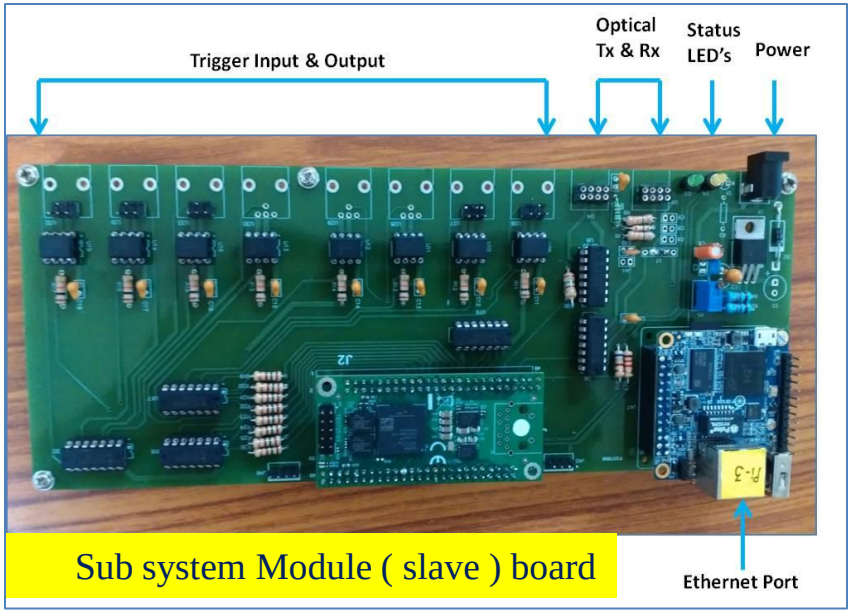


Central Module board

- Maximum Slave modules that can be connected = 8
- Synchronous & Shut down sequence event generation time resolution = 10 µS
- Event time stamp resolution = 1µs
- Maximum number of synchronous & shut down sequence events = 255
- Maximum event time stamp duration = 4294.96s (~ 71.58 min)



1U Rack mountable central module

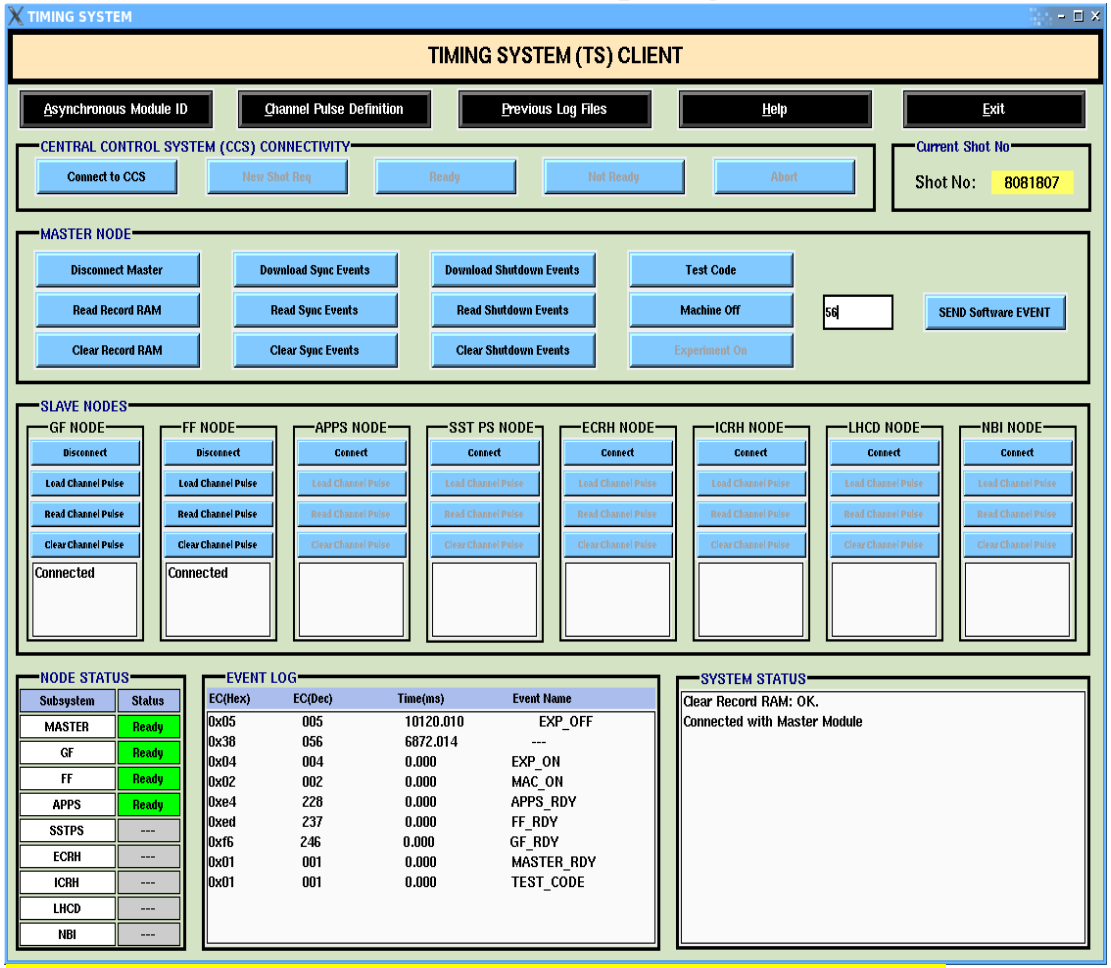


Sub system Module (slave) board

- TTL Channel Outputs = 8 (Low to High)
- TTL Channel Inputs = 8 (Rising edge i.e. low to high logic)
- Minimum pulse width for channel outputs = 1µS
- Maximum pulse width for channel output = 429.49 sec
- Minimum pulse width at channel input = 500ns (as event)
- Channel outputs for multiple events or same event

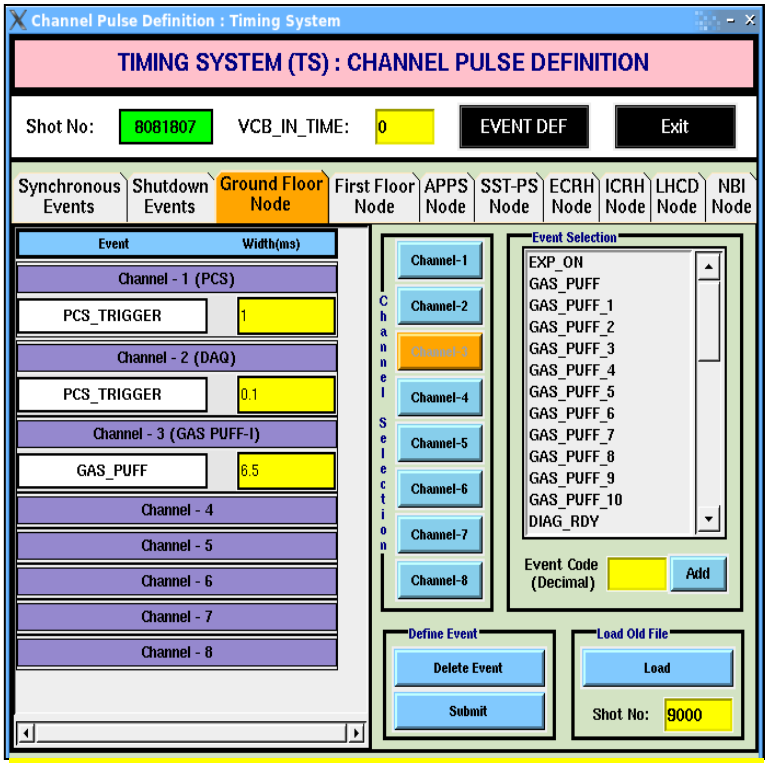
1U Rack mountable sub system module

Timing System Client application



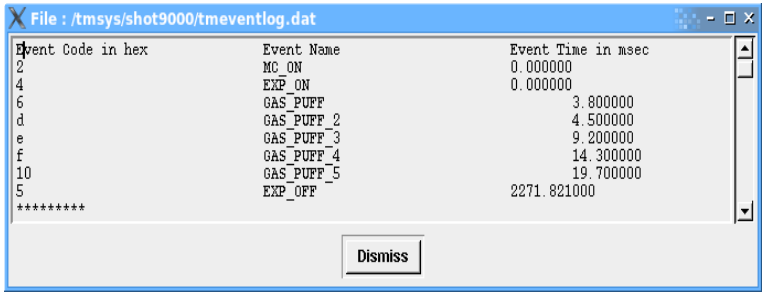
Timing System Client

- Linux based application
- Client-Server architecture
- Connects & Configures all Timing System modules
- Issues commands to generate experiment sequences
- Online event information to operator



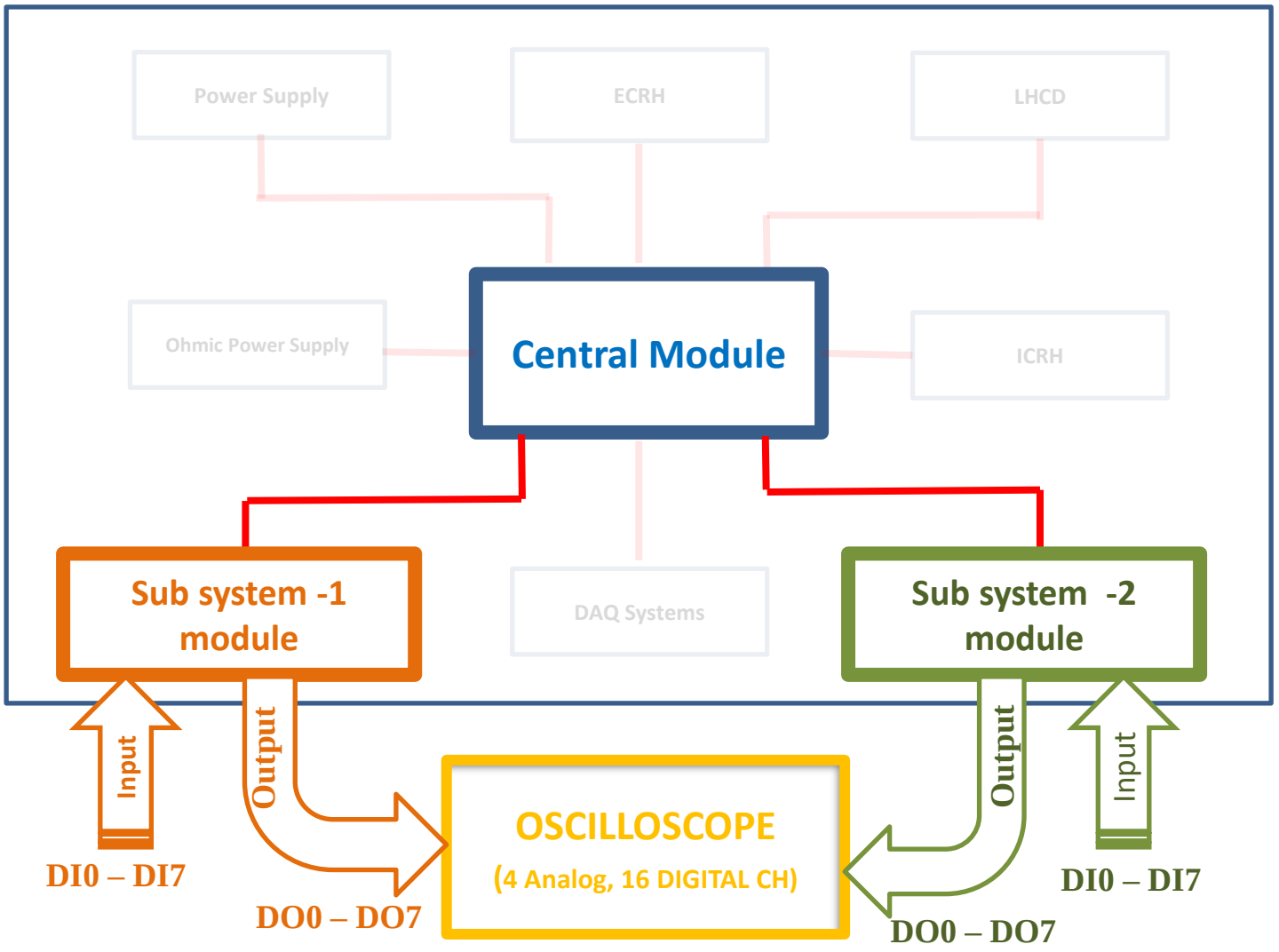
Channel Pulse Definition

- Configures experiment sequence
- Configures sub system modules for trigger pulse outputs



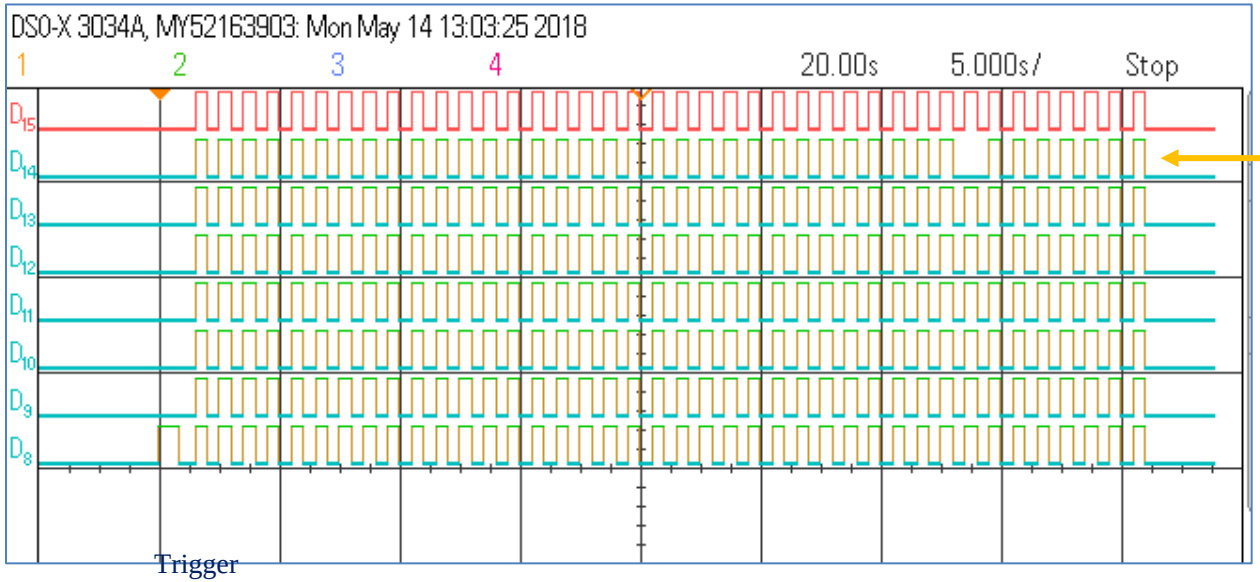
Event log

Timing System - Performance, Results & Validation



Set Up - Central Module (Master) – and Two Sub system modules (Slave)

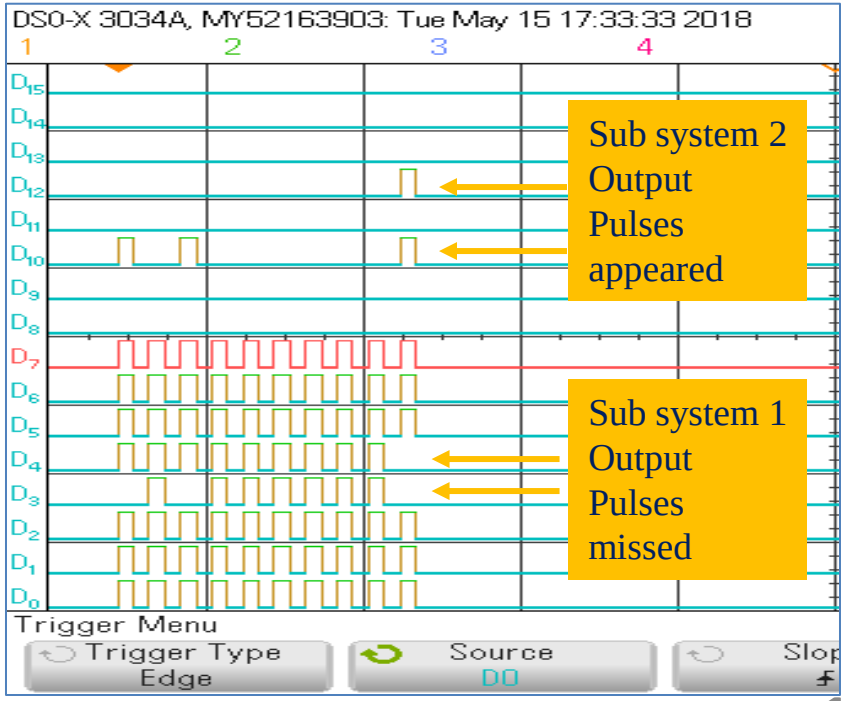
Performance, Results & Validation



Output Pulse missed

Sampling data bits (@ Receiver -16 x Bit rate)
But, only single sampling point to decode received data bit

Multiple sampling points with averaging – to decode received data bit



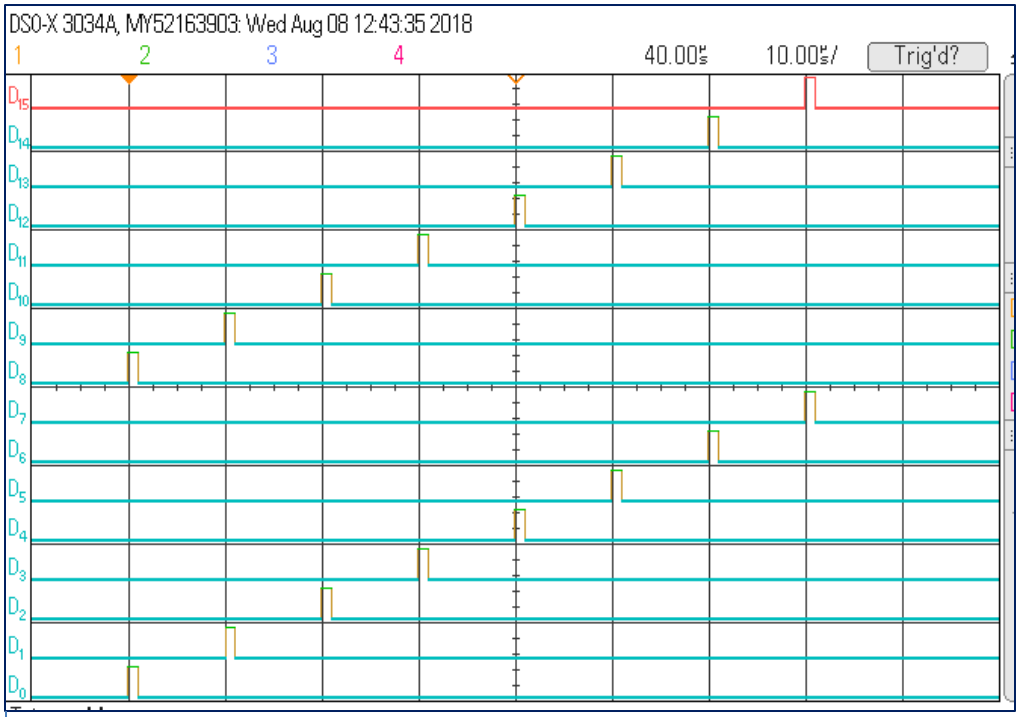
Sub system 2 Output Pulses appeared

Sub system 1 Output Pulses missed

Reference:(9)

Performance, Results & Validation

Central Module (Master) – Experiment events (Synchronous) sequence at resolution of 10 µs



Pulse outputs corresponding to Synchronous Events on Two sub systems
D0-D7 : Sub system1 outputs
D8-D15 : Sub system 2 outputs

Event Code in hex	Event Name	Event Time in msec
2	MC_ON	0.000000
4	EXP_ON	0.000000
c	GAS_PUFF_1	0.010000
d	GAS_PUFF_2	0.020000
e	GAS_PUFF_3	0.030000
f	GAS_PUFF_4	0.040000
10	GAS_PUFF_5	0.050000
11	GAS_PUFF_6	0.060000
12	GAS_PUFF_7	0.070000
13	GAS_PUFF_8	0.080000
14	GAS_PUFF_9	0.090000
15	GAS_PUFF_10	0.100000
5	EXP_OFF	2440.020000

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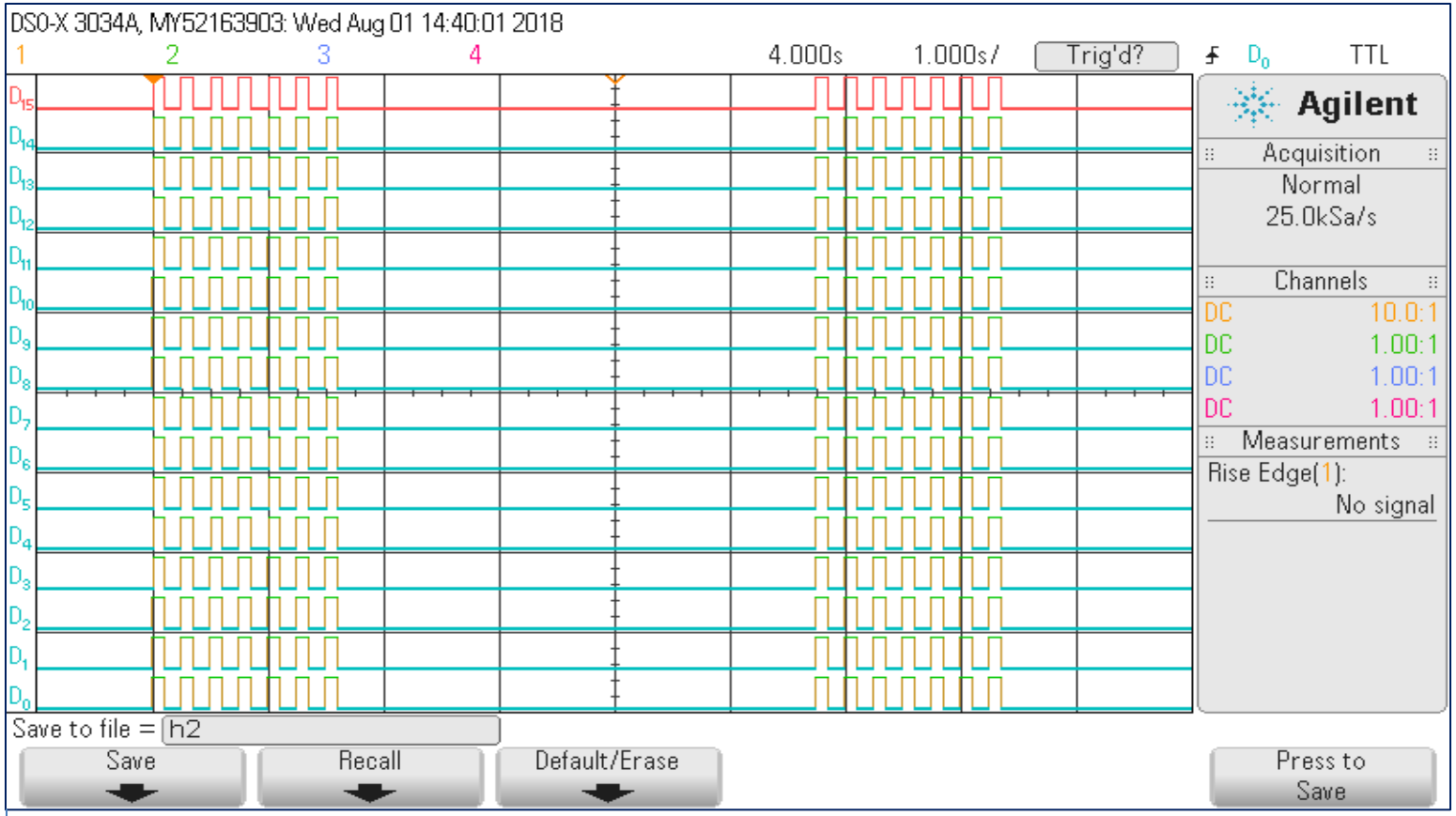
Event Log file

Performance, Results & Validation

Central Module (Master) – Experiment events (Synchronous) sequence test



Synchronous events at slaves- Generate pulse outputs on receiving synchronous events (7x8) and shutdown events (7x8) on all eight outputs of two different slave modules

D0-D7 : Sub system1 outputs

D8-D15 : Sub system 2 outputs

Performance, Results & Validation

Central Module (Master) board – Event log resolution of 1µs

Event Code in hex	Event Name	Event Time in msec
2	MC_ON	0.000000
4	EXP_ON	0.000000
f7	?	0.003000
ee	LHCD_LOOPBACK	0.003000
6	GAS_PUFF	1.000000
5	EXP_OFF	4320.049000

****

Event time stamp at Master – Two asynchronous events generated simultaneously by two slaves
(* Note – Sub system1 – Async event 0xf7
Sub system 2 – Async event 0xee)

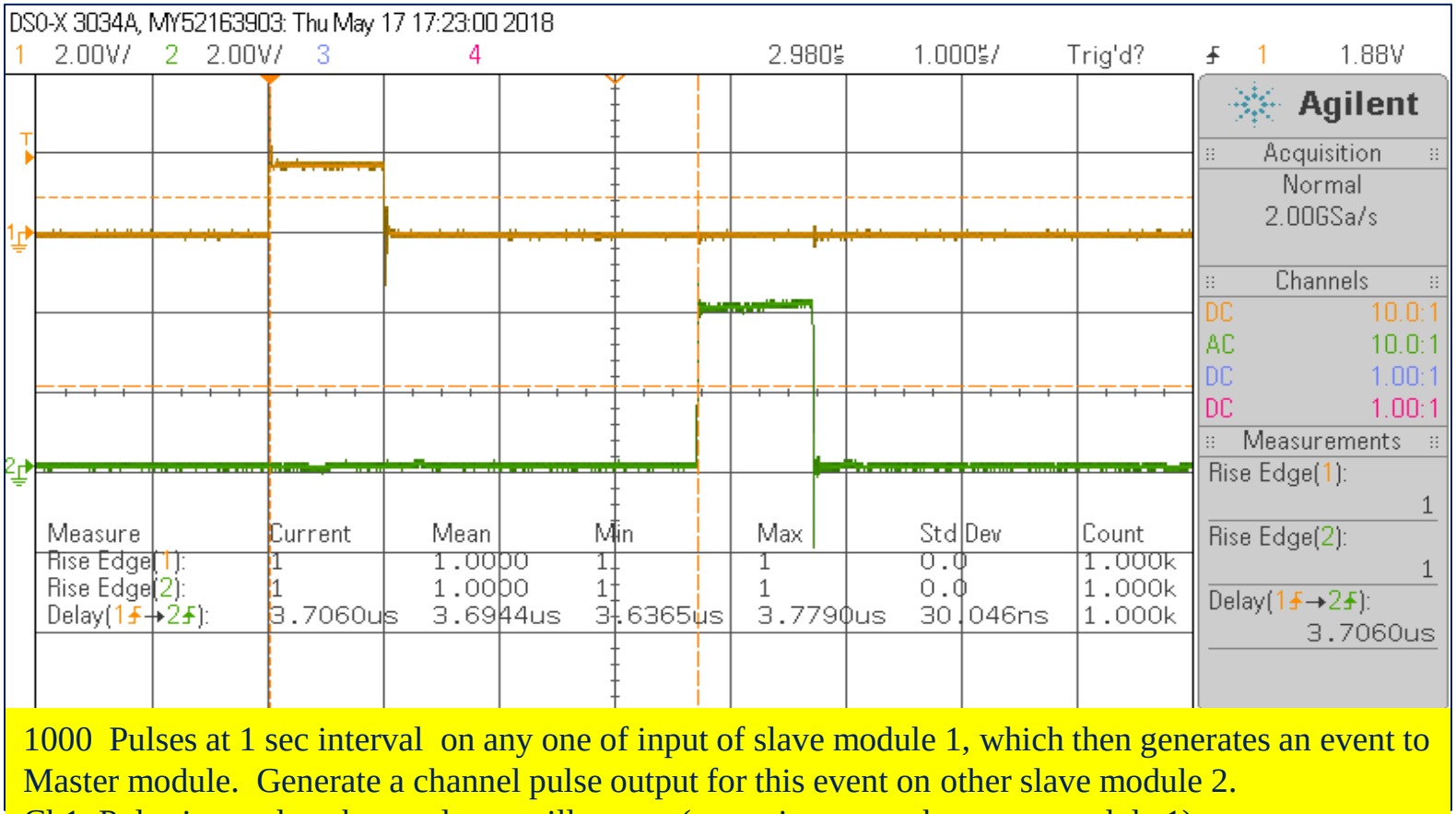
Event Code in hex	Event Name	Event Time in msec
2	MC_ON	0.000000
f7	?	4447.268000
f0	?	4447.268000
f9	?	4447.276000
ee	LHCD_LOOPBACK	4447.276000
f8	?	4447.284000
ef	?	4447.284000
fa	?	4447.292000
f1	?	4447.292000
fb	?	4447.300000
f2	?	4447.300000
fc	?	4447.308000
f3	?	4447.308000
fd	?	4447.316000
f4	?	4447.317000
fe	?	4447.324000
f5	?	4447.325000

****

Event time stamp at Master – 16 asynchronous events generated simultaneously by two slaves
(* Note –
Sub system1 – Async events from 0xf7 to 0xfe
Sub system2 - Async events from 0xee to 0xf5)

Performance, Results & Validation

Sub system Module – Event Latency Test on two different sub system modules (3m optical fiber)

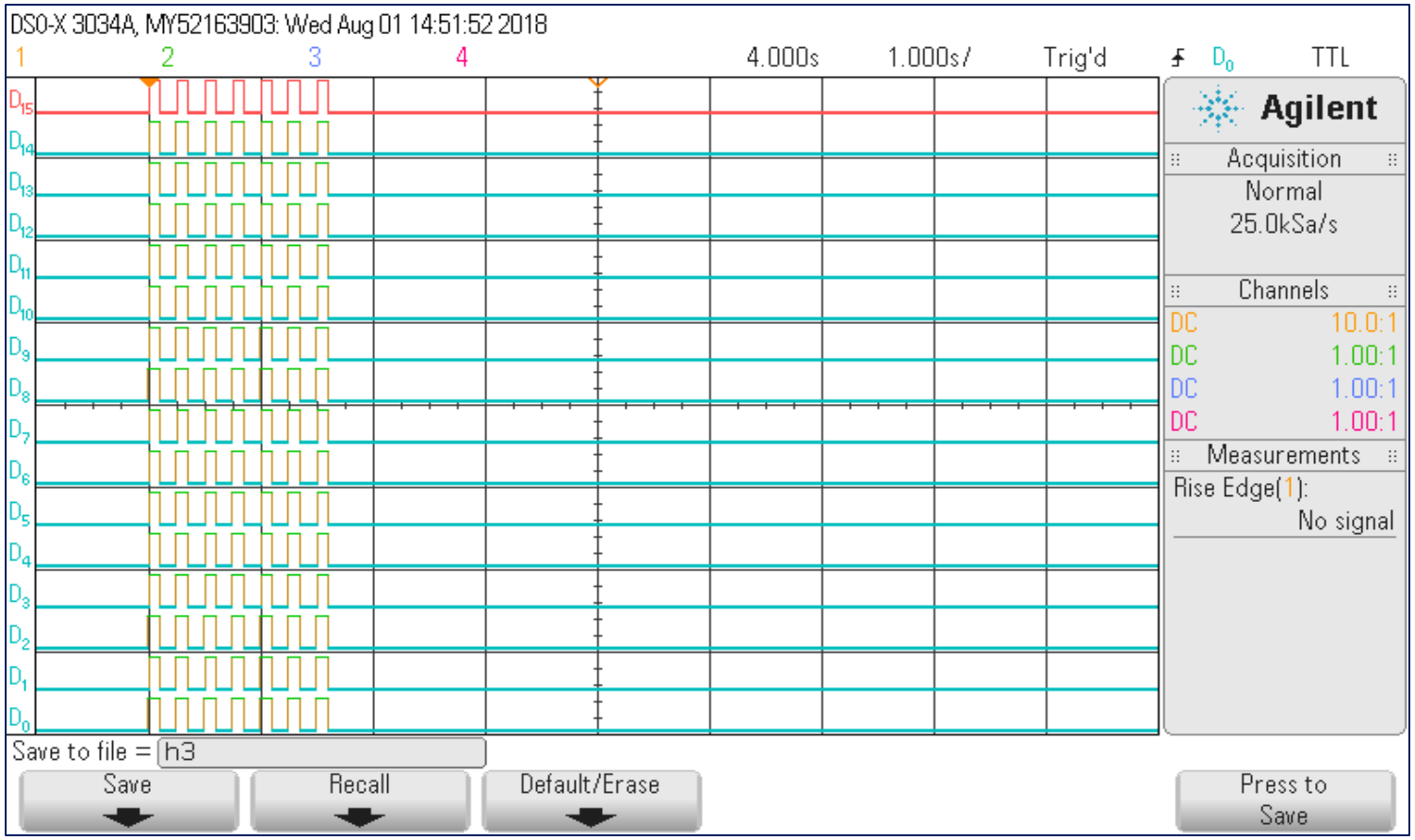


1000 Pulses at 1 sec interval on any one of input of slave module 1, which then generates an event to Master module. Generate a channel pulse output for this event on other slave module 2.
Ch1: Pulse input also observed on oscilloscope (as an input to sub system module 1)
Ch2: Output generated on sub system module 2 by the corresponding event generated due to above pulse input

#Note- Voltage level of Ch1 on oscilloscope is less, as it is measured across opto-coupler input.

Performance, Results & Validation

Sub system Module – Simultaneous Asynchronous events (3m optical fiber)

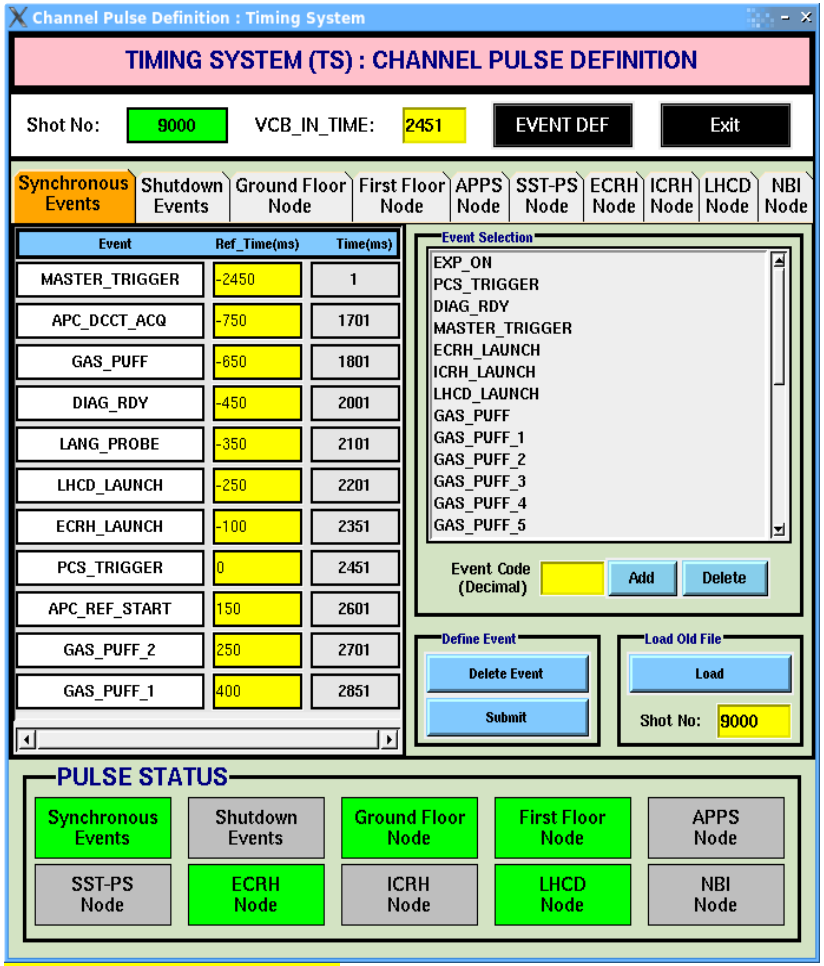


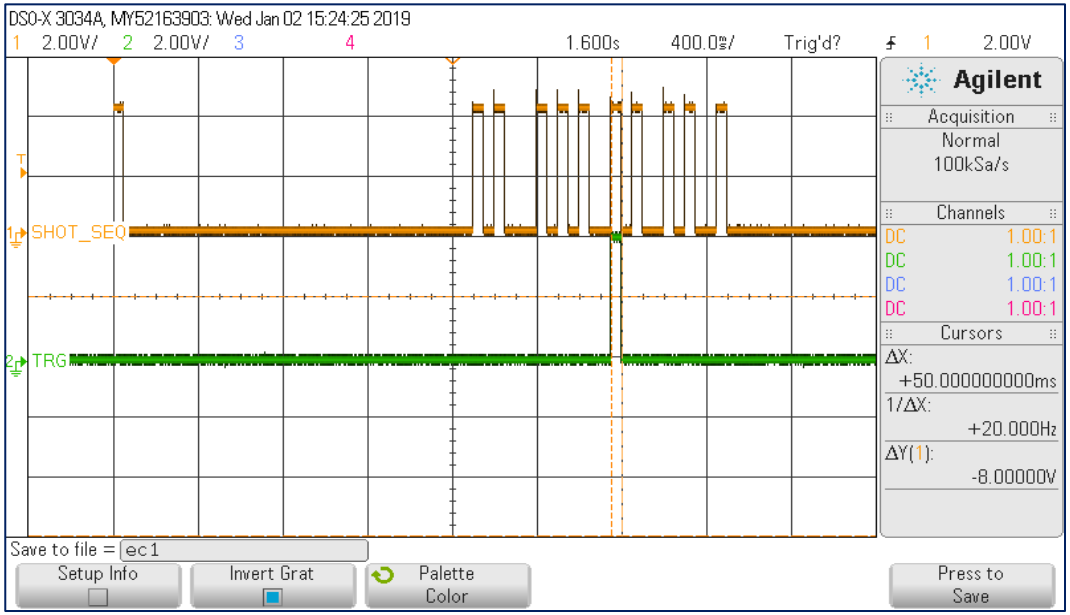
Asynchronous events - Generate asynchronous events by simultaneously applying 7 consecutive pulses on all eight inputs of two different slave modules. Configure pulse outputs for the generated asynchronous events.

D0-D7 : Sub system1outputs

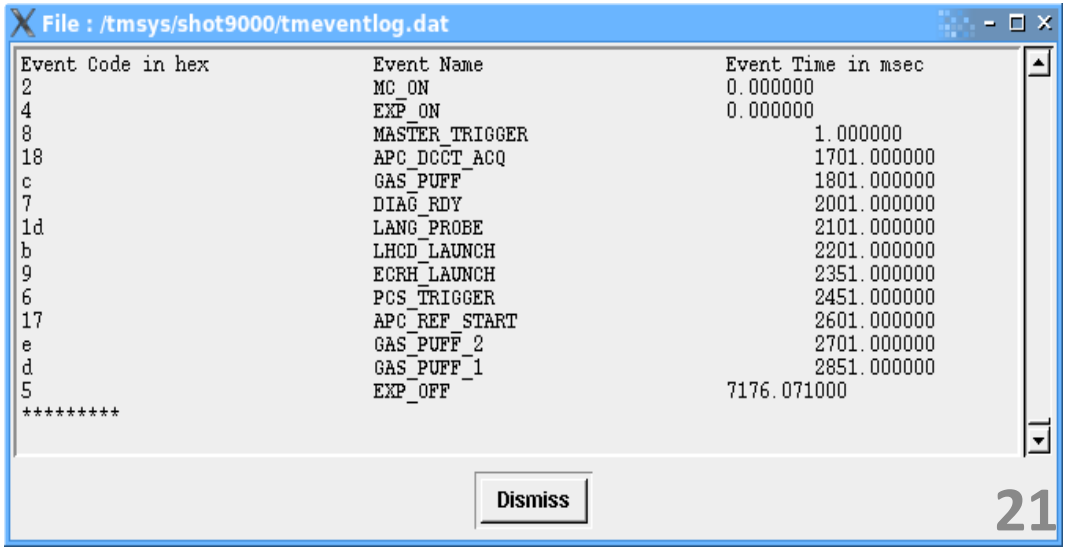
D8-D15 : Sub system 2 outputs

Field Testing – Similar to actual plasma shot scenario





Real time event sequence generation (ECRH Launch trigger in reference to actual plasma shot scenario)



Generate experiment sequence similar to actual scenario

Log file – registers all events with time stamp

New Timing System Cost (Estimations)

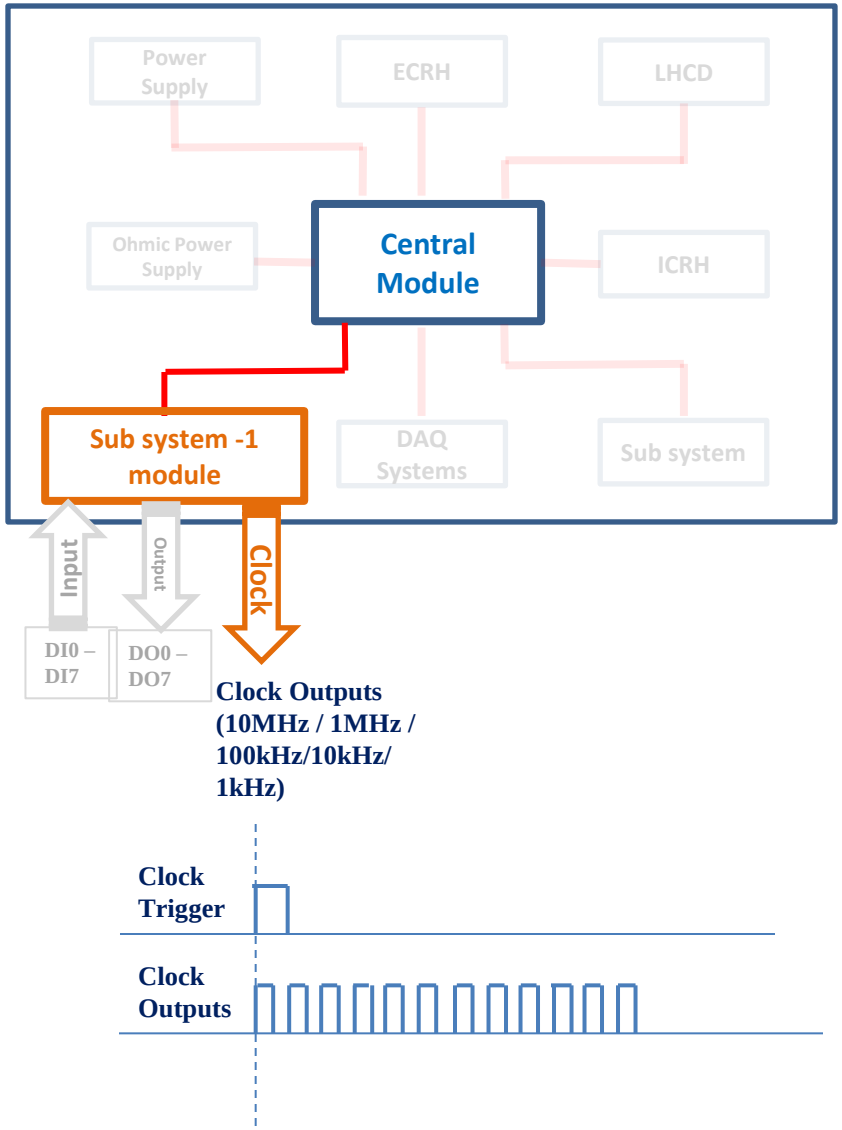
Central module (Per unit)	Rs. 41,698 /- approx. (600$)
Sub system module (Per unit)	Rs. 25,168 /- approx. (360$)
Timing System with 1 Central module and 8 sub system modules	Rs. 2,43,042/- approx. (3475$)

#Version1 - Module Costs* (Indian Rupees Rs)(U.S $)

 # Version 1 (Without Clock Synchronization & GPS IRIGB interface)

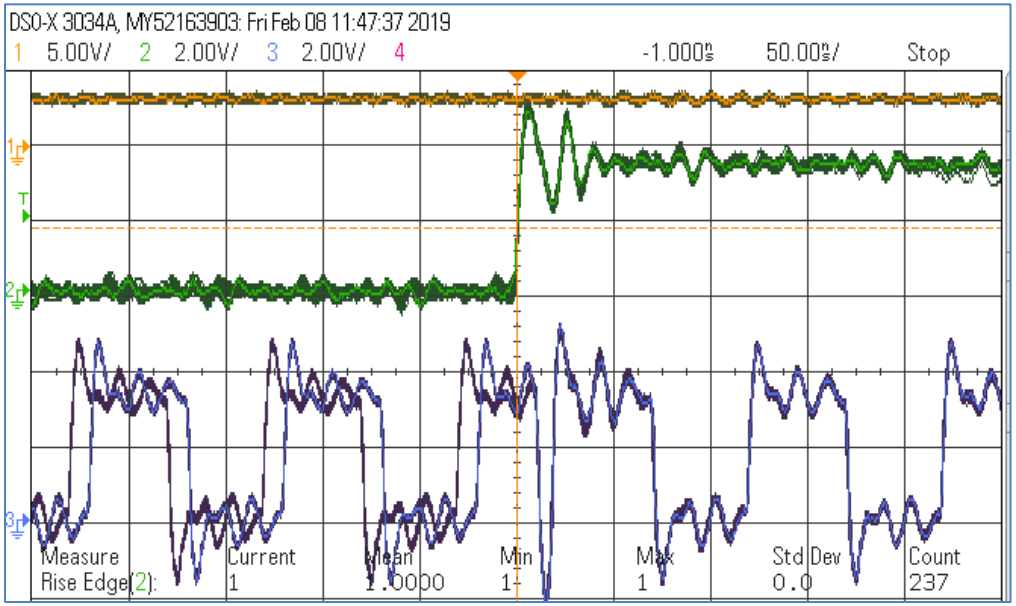
** Excludes the cost of material available with Institute for Plasma Research Stores department, Workshop, Job hours etc.*

Further Development - Clock Synchronization (In Progress)



Clock source under test	Frequency (MHz)	Stability (ppm)	CTE over 10 second	CTE over 60 second	CTE for 3600 second
Local Artix-7 oscillator SiT8008	100MHz	20 ppm	200 µs	1.2 ms	72 ms
OCXO-2050 (Old Timing System)	20 MHz	0.1ppm	1 µs	6 µs	360 µs
Proposed	20 MHz	0.02 ppm	0.2 µs	1.2 µs	12 µs

Clocks and their calculated Cumulative Time Errors (CTE)



Reference:(10)

Further Development - GPS IRIG-B Interface, Event prioritization, Error handling (In progress)

- Propagation delay compensation
- Event prioritizing logic at Central sub system module
- Error handling features (Parity, CRC …)
- Develop GPS IRIG-B interface for the modules. (For GPS synchronization and GPS time)

Summary

- A Platform independent, stand alone, 1U rack mountable timing system is designed, developed and tested.
- The performance test results are comparable and acceptable.
- The development cost is observed to be optimized considering the simple design adopted.
- Design can be implemented with other FPGAs (different make).
- New in-house design will be advantageous and it can be easily adapted for time synchronization applications in small, medium size tokamaks or experimental devices irrespective of hardware/ software platforms.

References

1) **Overview of time synchronization system of steady state superconducting tokamak SST-1 , 1A. Kumar, H. Masand, J. Dhongde et. al, Fusion Engineering and Design 112 (2016) 683–686**

2) **https://www.xilinx.com/products/silicon-devices/fpga.html**

3) **HFBR-14xxZ and HFBR-24xxZ Series (Broadcomm), Low-Cost, 820 nm Miniature Link Fiber Optic Components with ST®, SMA, SC and FC Ports - Data sheet**

4) **AFBR-24x8xZ(Avago Technologies) DC-50MBd Miniature Link Fiber Optic Receiver-Data sheet**

5) **Ultra-Compact UART Macros for Spartan-6, Virtex-6 and 7-Series, Ken Chapman, 29th March 2013**

6) **The Design of High Speed UART, J. Norhuzaimin and H.H Maimun, 2005 Asia Pacific Conference on Applied Electomagnetics Proceedings, December 20-21, 2005**

7) **FPGA Module with Xilinx Artix-7 XC7A35T (TE0725-03-35-2C), Trenz Electonic (https://shop.trenz-electronic.de/en/TE0725-03-35-2C-FPGA-Module-with-Xilinx-Artix-7-XC7A35T-2CSG324C-2x50-pin-header-3.5-x-7.3-cm)**

8) **http://www.orangepi.org/orangepizero/**

9) **UART Receiver Synchronization: Investigating the Maximum Tolerable Clock Frequency Deviation, Indian Journal of Science and Technology, Vol 10(25), July 2017**

10) **The AD9548 as a GPS Disciplined Stratum 2 Clock, Ken Gentile (Analog Devices – AN 1002 Application Note)**

Thank You