The Implementation and operation of the 4th version of the KSTAR Fast Interlock System

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ABSTRACT

- 4th version of KSTAR Fast Interlock System (FIS) using NI c-RIO technology built and operated in 2018.
- The EPICS irio driver enables complete control and monitoring of the FPGA, and the distributed interlock information can be integrated in the FIS IOC via EPICS .
- The FPGA, which is responsible for signal processing at high speed, implements the event counter logic to record the event occurrence time.
- The event generated in the FPGA is displayed in 10 microseconds resolution by the 100 kHz operation period.

INTRODUCTION

History of KSTAR FIS [1], [2]

- 1st Version, 2009 : Central Control System +Plasma Control System using RFM within 200ms
- 2nd Version, 2012 : Fast interlock interface + TSS
- 3rd Version, 2014 : 2nd Version + PFC, NB armor temp. faults
- 4th Version, 2018 : c-RIO+EPICS IOC

FIS protection logics [3]

- Ip protection logic : FPGA processing
- PCS, SIS interface logic : information transfer using hardwire
- EPICS PV interface logic : information transfer using EPICS PV

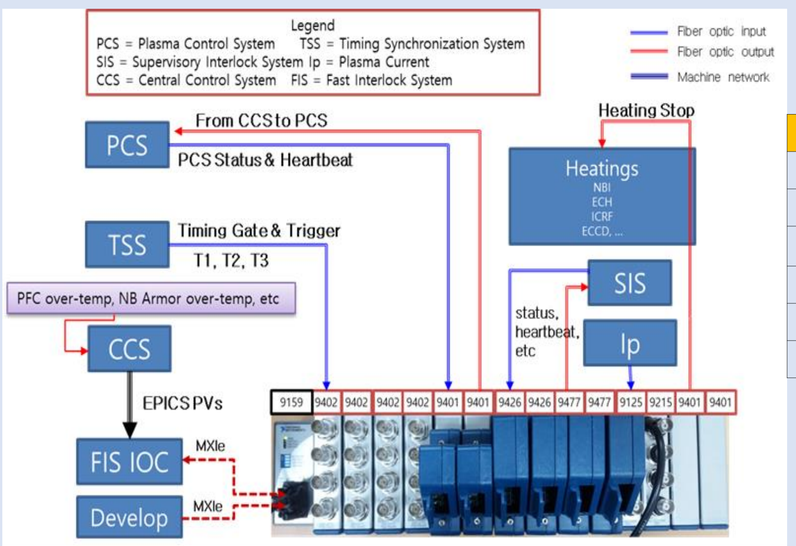
IMPLEMENTATION

FPGA Programming

- Labview FPGA module, EPICS irio driver [4]
- 4 execution loops (Ip logic, Event count, heating stop, heart-beat check)
- Timing sync. With KSTAR TSS

OPI

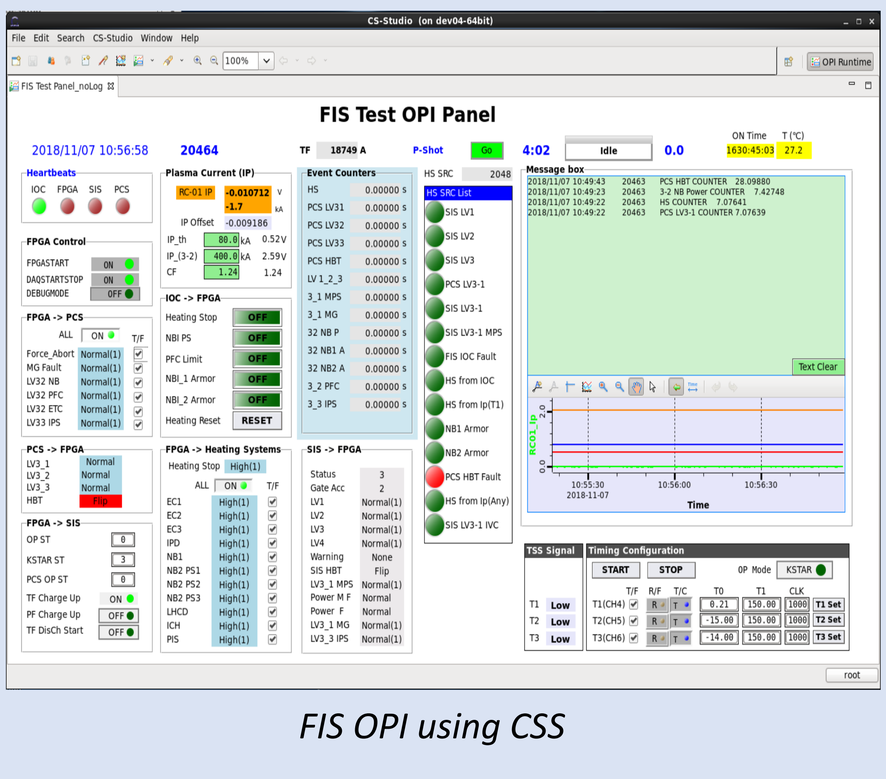
- Using EPICS Control System Studio(CSS)
- Linked with KSTAR shot based operation



Configuration and signal flows

Module	Description	No.	Related Sys.
NI 9159	14-slot chassis, LX110 FPGA, MXIe	1	FIS IOC
NI 9402	4-ch, 55ns, DIO, BNC	4	CTU
NI 9401	8-ch, 100ns, DIO, 25pin D-SUB	4	Heating sys. , PCS
NI 9426	32-ch, 7㎲, DI, 37pin D-SUB	2	SIS Input
NI 9477	32-ch,8㎲, DO, 37pin D-SUB	2	SIS Output
NI 9215	4-ch, 100kS/s/ch, 16 bit AI, BNC	2	RC01

C-RIO module datails



FIS OPI using CSS

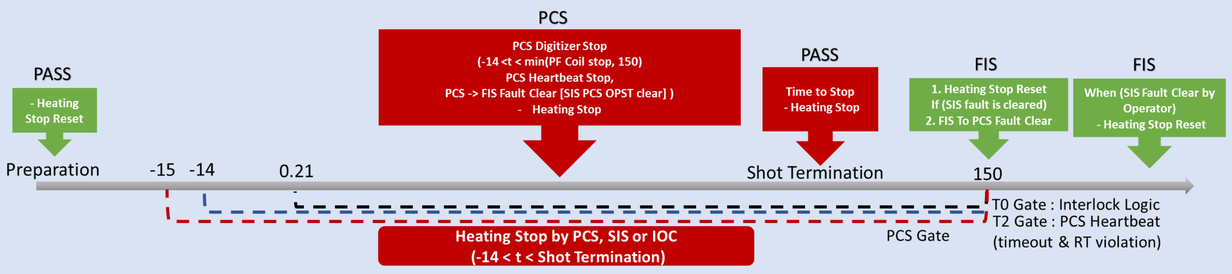
OPERATION and RESULTs

Reset and Clear faults

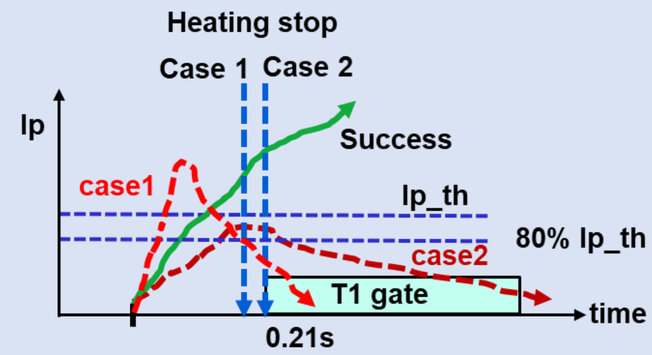
- Pulse Automation and Shot Scheduling(PASS), PCS, Timing interfaced FPGA logic.
- Least operator's intervention.

Performance Evaluation

- Focus on start-up phase (<250ms)
- Analysis on Ip profile and Heating Stop(HS) time
- Event counter value converted to Blip based discharge time.
- 100kHz Ip protection logic perfectly working and generated HS signal.
- Case1, case2 shows perfect working.

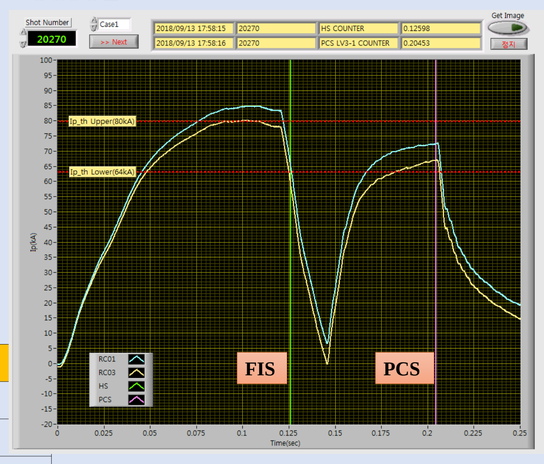


Reset and clear logic

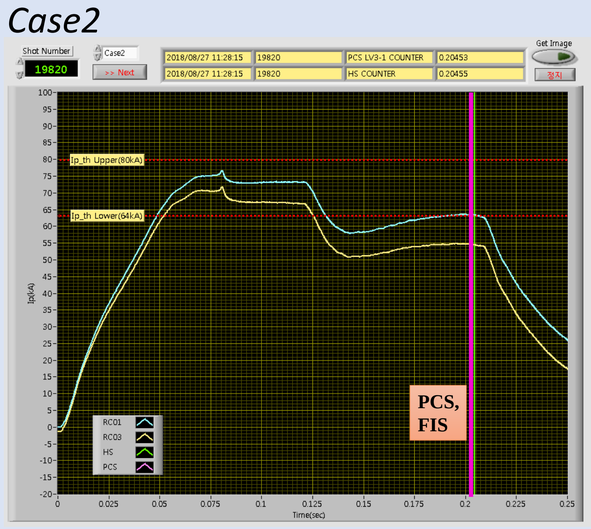


Ip protection logic

Case1



Case2



Ip protection examples

CONCLUSION

- 4th version of KSTAR FIS worked without any problem during 2018 operation.
- Using FPGA event counter logic, FIS performance evaluation was done.
- Event counter was very useful to specify the error/fault source.
- The level of Ip threshold should be reviewed and another protection logics can be added for the FIS upgrade.

REFERENCES

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2. J. Hong, et al., "Development and operation of fast protection for KSTAR", Fusion Eng. Des. 112, 2016
3. T. Tak, et al., "Plasma protection mudule design for ITER CIS fast architecture", Fusion Eng. Des. 124, 2017
4. "IRIO EPICS device support-V1.2.0 user's manual", UPM, Spain