RT AMPLITUDE CONTROL LOOP: TESTING OF R&D ICRF SOURCE AT HIGH POWER

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Abstract

Ion Cyclotron Heating and Current Drive (ICH&CD) system is an important auxiliary heating and current drive systems for ITER Tokomak machine. Source part of the ICH&CD system is to be delivered by Indian Domestic Agency IN-DA as in-kind contribution. One of the critical requirements of IC-RF source is to operate the amplifier at constant power for dynamic load conditions of VSWR 2:1 and able to match the requested power in 10ms time scale. To realize constant power requirement, an amplitude control loop is developed using NI make PXI-7841R & LabVIEW-FPGA module. The output power is controlled by changing the drive reference to vary output power of Solid State Power Amplifier (SSPA), which has in-built amplitude control loop. Further online variation of anode biasing voltage is incorporated in this amplitude control loop considering Screen Grid (SG) current as a controlling parameter. In this control loop, other parameters like Anode current and Anode dissipation are critically monitored and ensure constant output power by adjusting drive power and anode biasing voltage in real time. Considering reliable and safe operation, source will be forced to operate in power down mode by forcing internal reference generated by the amplitude control loop itself, if any operating parameter crosses maximum operational limit. Even if the power down mode is also not able to make operating parameter stable, local protection function initiate RF off sequence to protect the RF source. The paper describes test result of amplitude control loop along with flowchart of the algorithm and timing diagram.

1. INTRODUCTION

Ion Cyclotron Heating and Current Drive (ICH&CD) system is one of the important auxiliary heating and current drive systems for ITER experiment [1]. Initially 20 MW of IC power will be dumped to ITER plasma using 8 independent RF sources that can be operated in frequency range of 35-60MHz. To fulfil this requirement each ICH&CD source should be able to generate 2.5MW power. To finalize the final configuration of RF source, IN-DA has initiated R&D activity for Tetrode and Diacrode tube based amplifier system [2].

Each ICH&CD Source are made of two chain of RF amplifiers, combined together to generate 2.5 MW RF power. Each chain of amplifier is made of three stage cascaded amplifiers. These stages are: Solid State Power Amplifier (SSPA), Driver stage amplifier known as High Power Amplifier - stage 2 (HPA2) and Final stage amplifier known as High Power Amplifier - stage 3 (HPA3). The full configuration of ICRF source is shown in Fig-1. The critical requirements of IC-RF source is to operate the amplifier at constant power during dynamic load condition of VSWR 2:1 with any phase of reflection coefficient and is able to match the requested power in 10ms time scale. Also to operate high power amplifier, a proper sequence of operation has to be followed. The operation sequence of tetrode based amplifier emphasizes to make proper loading of the amplifier before applying screen grid biasing to the tube. If amplifier is lightly loaded (SG current is comparatively low), it shows oscillatory nature and cause arcing which terminate the RF pulse prematurely. Also it was observed that excessive screen grid current indicate generation of higher mode oscillation and if not treated properly & in timed manner, it may lead to failure of the tube. Considering all these operational constraints amplitude control loop is designed & developed using NI make PXI-7841R (LabVIEW-FPGA module) [3, 4].
2. AMPLITUDE CONTROL LOOP

To fulfill the ITER-requirement of RF source, Amplitude control loop is an essential part of local control unit of RF amplifier system. Main feature of Amplitude control loop is to take multiple inputs which are critical for the amplifier system and based on these input it will regulate the anode voltage as well as input drive. The critical parameters which are monitored continuously are SG current, anode voltage and anode current which defines anode dissipation. Basic configuration of the amplitude control loop is feedback control loop which take HPA3 output power as measurement reference and trying to match it with the requested power using PID controller. The output of PID controller acts as drive reference for Solid State Power Amplifier (SSPA) which has in-built internal power control loop. Further Screen Grid current is monitored continuously and if it crosses the defined limit, anode biasing voltage is increased to keep SG-current in predefined range.

2.1. Timing diagram: Characteristics of amplitude control loop

Characteristics of amplitude control loop are described using timing diagram shown in Fig.2. Timing diagrams are described in three parts; (a) the starting sequence of high power amplifier; (b) the action of amplitude control loop in dynamic load condition, which influences the SG current as well as Anode power dissipation (APD) and (c) the off sequence of amplifier. All the steps are numbered in the timing diagram as shown in Fig.2 and defined accordingly.

(a) Starting Sequence of the amplifier:

(1) As RF pulse is applied, predefined drive reference is passed as Proportional Integrator Derivative (PID) o/p to SSPA for maintaining the initial loading. After predefined time (50ms) SG is enabled which makes SG power supply ON and SG biasing voltage is applied to the tube. It is noted that overall response time of stabilising SG voltage is ~250ms.

(2) Amplitude control loop is activated at 300ms which enables the PID control loop and accordingly PID output is increasing in steps and checking APD as well as SG-current.

(3) As SG current crosses the user defined limit-1, anode voltage is increased in predefined steps keeping PID power reference constant. As anode voltage increased SG current decreases and becomes lesser than SG limit-1.

(4) As SG current is in limit, power reference for PID is increased to get required power. In this case PID output is increased and corresponding final output power is also increased which leads to SG current crossing the limit-1.

(5) As SG current crosses limit-1, anode voltage is increased to control it. As anode voltage is increased, final power is also increased and reaches to required power.
This indicates stable operation of amplifier which provides the demanded output constantly.

(b) **Action of Control Loop during Load Variation:**

(7) Influence of load variation SG current crosses limit-1, anode voltage is increased which may influence the output power but the output power is made constant through PID control loop and maintained the demanding power. This part of action comes under normal mode of operation of amplifier which defines the condition where demanded output power is made available by amplifier.

(8) As load is still varying in unfavourable condition which reflects on increasing SG current but anode voltage increment is not possible as it reaches to its maximum limit. Hence, reference of PID loop is decreased through the control loop and drags the system in limiting mode of operation where output power is limited and lesser than the requested power.

(9) As SG current is below limit-2 and anode dissipation is under control, limiting mode of operation continues.

(10) As anode dissipation crossing its defined maximum limit, anode voltage and PID reference is further decreased to make anode dissipation and SG current under limit.

(11) Control loop maintain the maximum possible output under limiting mode of operation.

(c) **RF OFF sequence of amplifier:**

(12) As RF starting sequence, off sequence is also maintained by this control loop. As time of RF on reaches the predefined off sequence timing, anode voltage and PID reference is decreased to initial starting level. This ensures proper loading and sufficiently low power to make switched off RF power.

FIG. 2. Timing diagram of amplitude control loop indicating different action
2.2. Flow chart for the algorithm developed for the control loop

Algorithm is developed to match the requirement defined by timing diagram which elaborate the characteristics of amplifier as defined above. FPGA coding is realized using LabVIEW FPGA module and code is burnt onto NI 7841R module. Control loop is running at user configurable time rate (default value is 200 microsecond). Also different parameters of control loop are passed to FPGA from graphical user interface through Real Time controller using RT-FPGA interface of LabVIEW. Algorithm is shown in Fig.3. LabVIEW PID toolkit is used in FPGA code. PID controller parameter are stabilized using Ziegler and Nicholas’ heuristic method.

![Flow chart - algorithm of Amplitude control loop](image)

*FIG. 3. Flow chart- algorithm of Amplitude control loop*
2.3. Test result of amplitude control loop

RF amplifier is tested at 55MHz with reference power of 1MW @ VSWR 1.5 with 90 degree reflection coefficient angle. The required initial loading for 13kV anode voltage biasing is ~150kW for HPA3, corresponding drive reference of 1V which is passed through LCU as power reference of SSPA. Fig.4 shows the oscillogram where control loop is activated after 300ms of RF pulse application and output power (Ch-2) is stabilized at 4.6V which corresponds to 1MW requested power within 170ms. PID output (Ch-1) is increased the drive reference of SSPA and anode voltage (Ch-4) is increased to keep SG current (Ch-3) within operational limit of 2.8A which is equivalent to 1.4V.

**Fig. 4.** RF ON sequence and response time of amplitude control loop

Fig.5 shows the oscillogram of RF OFF sequence where RF OFF initiating time is user configurable (set as 1sec). Before 1 sec of completing RF pulse, RF OFF sequences is initiated and hence drive reference of SSPA & anode voltage is reduced to staring value within 100 ms and remains stabilized. After completion of 1 second RF pulse is terminated and all measurement parameter becomes zero.

**Fig. 5.** RF OFF response time
Fig. 6 shows the oscillogram of complete RF shot of duration 8 second with flat top ~6 second where RF output power is constant at 1MW under influence of the control loop.

Fig. 7 shows the oscillogram of control loop response during variable load condition. Load is changed from VSWR 2 to 1 and again from VSWR 1 to 2 where electrical length of stub in mis-match transmission line is changed between 500mm to 1000mm keeping line stretcher at fixed position of 1000mm. It is clearly seen that anode voltage is continuously increased to bring down the SG current in operational limit defined as 1.6A which is equivalent to 0.8V. As load is changing in slow time scale, slight increase of SG current is detected by control loop and increase anode voltage in minimum defined step of 160V which corresponds to 0.1V defined by operator. Once SG current starts decreasing, output power is stabilized at 600kW which corresponds to 3.6V. Initial part of the oscillogram is pre-test shot of 10s for finalizing the configuration parameters.
3. LIMITATION & FUTURE PLAN

The achieved amplitude control loop time is ~200ms which should be reduced to 10ms time scale. The limiting factor is time response of SSPA. Existing SSPA has its own power control loop which maintain the output power constant (Band flatness < 1dB) throughout the frequency band of 35-65MHz. Overall response time of SSPA is 4-5ms. Also the Anode power supply response time is in the order of 2-3ms [5]. As step size for increment of reference drive power and anode voltage are kept minimum to keep control loop stable, loop will run many times to fulfil the requirement. The cumulative effect of these two sub-systems make response time of the control loop slower.

In future the control loop should be further optimized using FlexRIO FPGA architecture and by improving the anode power supply response time. Further improvement is expected if open loop SSPA along with voltage controlled attenuator is used to drive amplifier chain.

4. SUMMARY

Complex control logic is successfully implemented using NI make FPGA module. High power (~1MW) performance of the amplifier system with amplitude control loop for CW operation (~10s) is successfully demonstrated. Also the response of the control loop with dynamic load condition at 600kW is successfully demonstrated.

REFERENCES