TIMING AND SYNCHRONIZATION FOR INTEGRATED OPERATION OF LARGE VOLUME PLASMA DEVICE


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Abstract

The Large Volume Plasma Device (LVPD) is a cylindrical shaped, linear device (L=3 meter, \( \phi =2 \) meter) dedicated in carrying out pulsed plasma experiments (\( t_{\text{pulse}} \sim 9.2 \) ms) relevant to fusion and Magnetospheric plasma. In the recent past, investigations are switched from active wave plasma investigations to the understanding of plasma turbulence of whistler and Electron Temperature Gradient (ETG) nature, relevant to Magnetospheric and fusion plasmas. In LVPD, efforts are in progress towards enhancing plasma duration from existing 9ms to 50ms in order to cater need of carrying out controlled experiments on ETG turbulence, a major source of plasma loss in fusion devices by using variation in density gradient scale lengths. For this purpose, a centralized machine control system (MCS) for LVPD using LabVIEW is under development, which will provide timing and synchronization to the operation of different subsystems. The timing and synchronization of the heterogeneous I&C modules in terms of centralized clock, trigger, timing and interlocking is critical. The configured MCS consists of: (a) PXI based high end instrumentation system for diagnostics data acquisition, (b) Process automation system for automated control of sub-system’s operation and (c) data handling system. This paper discusses (a) state of art techniques for timing and synchronization of large physics experiments, (b) centralized timing and synchronization schema, (c) multi-module PXIe system’s clock synchronization on multi-segment bus, (d) timing and synchronization requirements of high current pulsed power supplies.

1. INTRODUCTION

An important consideration of the data acquisition and control system for a large physics experiment is the measurement accuracy and synchronization of measurements and control hardwares. Typically, such system needs high sampling measurements (MHz-GHz), high channel counts, complex timing and synchronization requirement and stability under harsh environmental conditions. The clock error [1] affects measurement accuracy and if it has an error, then the acquired signal reflects that error and reconstruction is not proper which lead to wrong interpretation of physics results. The experimental environmental factors which contribute to the clock errors are variation in temperature, aging, supply voltage, shock, vibration etc. The clock error is characterized by accuracy (in ppm), stability and jitter. Typically, clock is generated by an oscillator such as voltage-controlled (VCXO), Oven-controlled (OCXO) and Direct Digital Synthesis (DDS). In VCXO, the device tunes the output frequency by applying a DC voltage to the oscillator therefore performance is highly dependents on temperature. In OCXO, applied voltage controls the output frequency while maintaining on board temperature constant. DDS outputs stable clock in the frequency range from Hz to GHz range with sub micro-second accuracy using digital synthesis. Therefore, backplane clock of instrumentation bus should be extremely stable for tight coupling of I&C boards.

Large plasma physics devices offer challenging environment for engineers to design a measurement and control system. Large Volume Plasma Device (LVPD) [2] is a pulsed plasma device (\( T_{\text{discharge}} \sim 9.2 \) ms), having cylindrical vessel (L=3 meter, \( \phi =2 \) meter) and dedicated to the laboratory plasma experiments oriented towards the electron temperature gradient driven plasma turbulence and transports studies [3]. The device was operating with a VXI based data acquisition unit [4] hosted by a PC and manual process controls and presently undergoing a major upgradation of its subsystems and capabilities. New machine control system (MCS) is under development. It consists of: (a) Process automation system [5] for automated control of sub-system’s operation, (b) PXIe based data acquisition unit for plasma diagnostics [6] and (c) data handling system. The architecture of the machine control system is described in Figure 1. Acquisition unit 1 refers to PXIe based data acquisition unit, having high sampling 40 channels distributed over six boards. The data acquisition requirements come from (1) resident diagnostics (MHz sampling) and (2) fast diagnostics probes for fluctuating plasma parameters measurement (GHz sampling). Acquisition unit 2 refers to the VXI based data acquisition unit. A process automation system (PAS) has also been under development and currently integrates (a) filamentary cathode heating power supply and (b) probe positioning system (12 stepper drive based electro-mechanical assemblies) and under active enhancements for other operational processes. Data handling system provides integration of all
the system data at central location. Local data storage hard disk on PXIe archives the diagnostic data during plasma pulses. A RAID based data server (HP DL 360 Gen9) is procured for implementation of data handling system for centralized data archival.

![LVPD machine control system architecture](image)

**Figure 1 LVPD machine control system architecture**

MCS is a multi-controller and multi-board data acquisition and control environment and synchronous orchestration of all controllers and I/O modules is a must for machine exploitation for physics investigations. Currently, the timing and synchronization requirements are followings:

a. Multi module synchronization on PXIe: it includes synchronization of backend clock and I/O board’s oscillators, trigger and pulse generation and propagation over backplane etc.
b. Timing and Synchronization requirements for process automation of various power supplies under procurements.
c. Timing and synchronization for data handling and archival.

Section 2 describes the conventional techniques of timing and synchronization, architecture of PXIe bus, specialized hardware and software solutions used. Section 3 discusses the obtained results and concludes the discussion.

2. LITERATURE SURVEY

MCS has multi-controller and multi-module architecture. Therefore, we need signal as well as time based synchronization. Timing and synchronization techniques are classified into two categories as represented in Figure 2. In signal based synchronization, clocks and triggers are physically connected between systems. It is highest-precision synchronization and accuracy achievable with this technique is tens of nanosecond. In time based synchronization, multiple systems are synchronized with the common time base and events. Trigger and clocks can be generated based on this reference as time stamped and correlated in post processing. The time
synchronization protocols (GPS, IEEE-1588, IRIG-B etc.) coordinate events at large distance typically greater than 10m and the achievable accuracy is under 100 nanoseconds.

Recently a PXIe based data acquisition unit has been procured, programmed and commissioned. PXIe is the latest addition to the PXI bus which increases backplane bandwidth from 132MB/s to 6GB/s and also provides advanced timing and synchronization features. It offers the lowest latency of all mainstream commercial I&C bus technologies. The architecture of the PXIe [7] is represented in Figure 3. It maintains 10 MHz and 100 MHz (differential) clock along with various trigger lines for inter-module triggers and clock routing. The backplane clock can also be provided externally by timing slot and phased locked for signal integrity and to maintain phase noise performance.

Figure 2 Spectrum of timing and synchronization techniques in terms of proximity to source and time accuracy (refer [7])

Figure 3 PXIe bus architecture showing trigger and clock lines for timing and synchronization (refer[8])

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The data acquisition unit has 40 channels which are spread over six data acquisition boards. It needs signal based synchronization over backplane among all boards using centralized and stable clock shared among all hardware board and phased locked. We also need routing of trigger for simultaneous triggering of multiple analogue input boards at the same instance. Table 1 shows the hardware configuration and clock sources of procured data acquisition unit. It can be observed that the clock source type is VCXO (which has high temperature dependence) for all hardware modules with ppm level accuracy.

| Table 1PXIe based data acquisition unit hardware |
|-----------------|-----------------|-----------------|
| Board           | Make            | Clock source,   |
| Chassis (19 slot) | NI-1085 | VCXO at 10MHz and 100MHz,25ppm Chassis clock |
| Controller (intel i7) | NI PXIe 8135 | VCXO at 2.5 GHz, 25ppm |
| DAQ board type 1 | NI PXIe 5164 (2 board installed) | VCXO at 60MHz, 25ppm |
| DAQ board type 2 | NI PXI 5105 (4 board installed) | VCXO at 60MHz, 25ppm |
| Hard disk and interface board | NI 8266 and NI PXIe 8384 (1 board installed) | Chassis clock |

Based on market survey, advanced timing and synchronization module NI PXIe 6674T [9] has been procured and installed in PXIe timing slot (Slot number #10) for synchronization of acquisition boards. It is a software configurable board which provides following facilities.

a. Generate and propagate PXI timing and trigger signals between boards in a PXIe chassis, between PXI chassis and between PXIe and Non-PXIe system.
b. Equipped with OCXO oscillator (5ppb accuracy) for synchronization and phase locking of the backplane clock and clock of all the modules by overriding built-in 10 MHz reference clock.
c. Equipped with DDS clock generator to generate clock from 0.3 Hz to 1 GHz with micro-hartz resolution.
d. Equipped with configurable 6 numbers of programmable function interface (PFI) lines (PFI 0..5) or 3 number of differential LVDS lines (LVDS0..2) as either input or outputs which can be used for signal terminals or routing.

The MCS is based on the LabVIEW [10] software development platform. NI sync library [11] of LabVIEW is used for configuration and interfacing of timing and synchronization card. It provides low level routines. We have developed object oriented application wrapper on it for integration as well as a test application for the use of NI 6674T board.

3. RESULTS AND DISCUSSIONS

We have developed a graphical user interface, which facilitates: (a) generation of signals (continuously or burst of pulses), (b) phase locking of chassis clock and OCXO clock of 6674T board and (c) routing of signals. The burst of pulses define the discharge duration and acquisition timings. The continuous clock can be used as sampling clock input to the acquisition cards of MCS. These pulses can be synchronously transferred on the PXIe internal trigger lines or output terminals (PFI0 to PFI5) leading to the reduction in number of connections. We can also generate maximum up to six correlated signals of frequencies (f) and frequency divided by an integer factor (e.g. f/2). DDS clock source can generate maximum clock frequency up to 1.25 GHz. Figure 4 represents the developed user interface. Phase locking loop status between PXI chassis and OCXO can be observed on developed software as well as ACT and ACC LED’s colour on timing and synchronization board.
We have compared of the phase between OCXO clock and backplane clock available from a terminal on chassis. Figure 5 represents the scenario, when both the clocks are not phase locked and observed phase delay between them is $237\,^\circ$. Figure 6 represents the scenario, when both are phase locked and observed phase delay between them is $10\,^\circ$. The measurements are taken on the NI scope software provided with NI high speed digitizers (NI 5162 digitizer card) using the 100 nanosecond/division time scale. Further improvement of this time scale is not feasible due to restrictions on the configuration setting of digitizer card.
Figure 5 It represents a scenario of phase comparison between OCXO (CH0) and backplane clock (CH1) when they are not in phase lock loop. We can observe a phase delay of 237°. The time base is represented in 100ns/Div on NI scope soft panel sampled using NI 5162 (1.25 GS/s) acquisition card.

Network time protocol (NTP) is used for synchronization of time across networked PCs (or controllers) in sub milli-second (or better) time scales. Recently, we have procured HP DL360 Gen9 server as central server based on Redhat Enterprise Linux (RHEL) server operating system (v7.2). NTP server software has been configured on RHEL operating system and work as a time server for all controllers of MCS. Recently, automation of filament power supply (20V, 10kA) for cathode heating and probe positioning system (12 electro-mechanical systems based on stepper drives) have been carried out on standalone PC. The procurement of an industrial PC for process automation is under process and deployed system will be synchronized with NTP server soon. The automation of other subsystems is also initiated and procured hardware controllers will also synchronized with NTP system.

LVPD is focusing on controlled ETG experiments. Hence, the procurement of two new power supplies for enhancing operational pulse duration from 9.2ms to 50ms has been initiated: (a) Discharge power supply (1 kA, 150VDC, 10ms ≤ T_{on} ≤ 50ms) for glow discharge and (b) Solenoid power supply (2.5kA, 170VDC, 10ms ≤ T_{on} ≤ 55ms) to power electron energy filter subsystem. These power supplies will be operated in individual as well as combined operational mode. The automation of these two power supplies for remote operation also lies in mandate of central control system. The procurement of the power supplies is under progress. The central control system will generate required timing pulses and control signals for operation of each power supply. In combined operation mode, solenoid power supply operation pulse will precede discharge power supply pulse (by 2-3 ms). Both the power supply will be operated during heated filamentary cathode operation. The specification and conceptual schema have been worked out and automation hardware procurements will be initiated soon.

In conclusion, we envisage this development as a step forward towards improvising the accuracy of the fast measurements in LVDP system by signal based synchronization of all data acquisition modules. The capability of data acquisition system in LVDP will be enhanced by including the time-based synchronization. A schema of which is also presented in this paper.
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